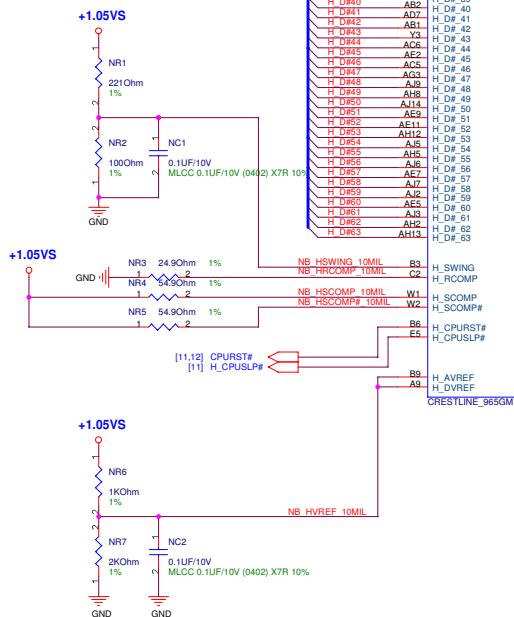


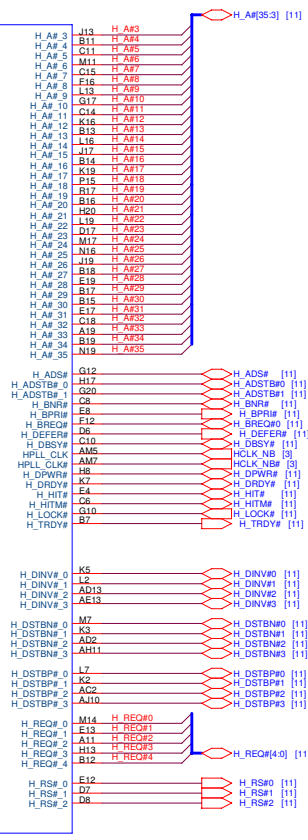


(PM965)  
(GM965)



## NU1A

## HOST



Z37S 12



**Title :** NB-965GM1-FSB

ASUSTek Computer INC

Engineer: *STD*

Size	Project Name
Custom	<b>STD</b>

Rev	2.0G
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Date: 星期四, 四月 26, 2007 Sheet 4 of 60



X P36	RSVD1
X P37	RSVD2
X R35	RSVD3
X N35	RSVD4
AR12	RSVD5
AR13	RSVD6
AM12	RSVD7
AN13	RSVD8
X J12	RSVD9
AR37	RSVD10
AM36	RSVD11
AL36	RSVD12
AM37	RSVD13
X D20	RSVD14

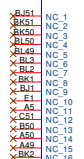
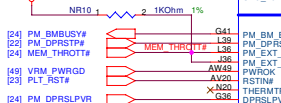
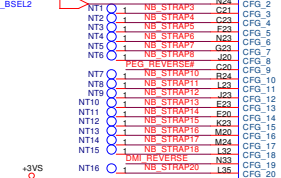
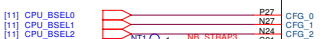
**PEG\_REVERSE#**



LOW = N  
HIGH = I

NR9  
1KOhm  
1%  
X

DMI REVERSE



CRESTLINE 965GM

RSVD

## JIXING

DDH

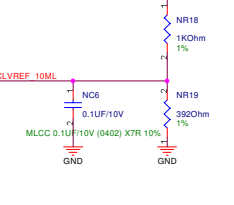
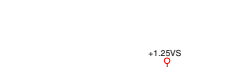
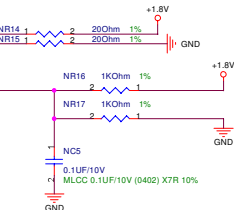
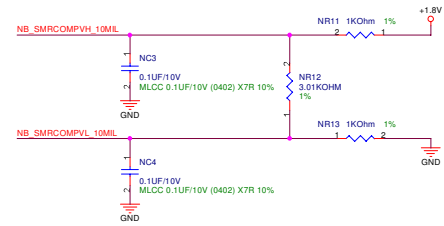
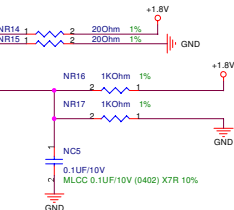
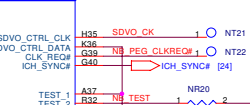
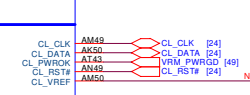
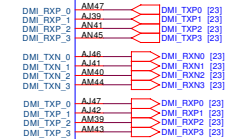
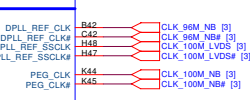
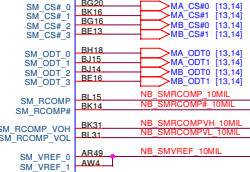
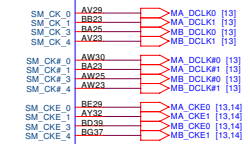
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DML	
CFG	

4

ME

MISC



**ASUS**® Title : NB-965GM2-DM/MISC

ASUSTek Computer INC. Engineer: STD

Size	Project Name
A3	STD

Date: 星期四, 四月 26, 2007	Sheet 5 of 6
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		<b>Title</b> NB-965GM3-PEG/VGA	
<b>ASUSTek Computer INC.</b>		<b>Engineer:</b> STD	
<b>Size</b> A3	<b>Project Name</b> STD	<b>Rev</b> 2.0G	
Date: 星期日, 四月 26, 2007		Sheet	6 of 60



[13] MA\_D[8:0]

## NU1D

MA D0	AB43	SA DQ 0
MA D1	AW44	SA DQ 1
MA D2	BA45	SA DQ 2
MA D3	AB46	SA DQ 3
MA D4	AB41	SA DQ 4
MA D5	AB45	SA DQ 5
MA D6	AT45	SA DQ 6
MA D7	AW47	SA DQ 7
MA D8	BB48	SA DQ 8
MA D9	BF49	SA DQ 9
MA D10	BA44	SA DQ 10
MA D11	BA45	SA DQ 11
MA D12	BB47	SA DQ 12
MA D13	BB50	SA DQ 13
MA D14	BB49	SA DQ 14
MA D15	BE49	SA DQ 15
MA D16	AW44	SA DQ 16
MA D17	BE44	SA DQ 17
MA D18	BB45	SA DQ 18
MA D19	BE40	SA DQ 19
MA D20	BE44	SA DQ 20
MA D21	BB45	SA DQ 21
MA D22	BB40	SA DQ 22
MA D23	BE40	SA DQ 23
MA D24	AB40	SA DQ 24
MA D25	AW40	SA DQ 25
MA D26	AT39	SA DQ 26
MA D27	AW39	SA DQ 27
MA D28	AW41	SA DQ 28
MA D29	AV41	SA DQ 29
MA D30	AV38	SA DQ 30
MA D31	AT38	SA DQ 31
MA D32	AT13	SA DQ 32
MA D33	AT13	SA DQ 33
MA D34	AW11	SA DQ 34
MA D35	AV11	SA DQ 35
MA D36	AU13	SA DQ 36
MA D37	AT11	SA DQ 37
MA D38	BA13	SA DQ 38
MA D39	BA11	SA DQ 39
MA D40	BE10	SA DQ 40
MA D41	BD10	SA DQ 41
MA D42	BD10	SA DQ 42
MA D43	AY9	SA DQ 43
MA D44	BB10	SA DQ 44
MA D45	AW9	SA DQ 45
MA D46	BB9	SA DQ 46
MA D47	BB9	SA DQ 47
MA D48	BB5	SA DQ 48
MA D49	AY7	SA DQ 49
MA D50	AT5	SA DQ 50
MA D51	AT5	SA DQ 51
MA D52	AY8	SA DQ 52
MA D53	BB7	SA DQ 53
MA D54	AB5	SA DQ 54
MA D55	AB8	SA DQ 55
MA D56	AB8	SA DQ 56
MA D57	AN3	SA DQ 57
MA D58	AN3	SA DQ 58
MA D59	AN10	SA DQ 59
MA D60	AT9	SA DQ 60
MA D61	AN8	SA DQ 61
MA D62	AM9	SA DQ 62
MA D63	AN11	SA DQ 63

CRESTLINE\_965GM

DDR SYSTEM MEMORY A

SA BS_0	BB19	MA_BA0 [13:14]
SA BS_1	BB19	MA_BA1 [13:14]
SA BS_2	BF29	MA_BA2 [13:14]
SA_CAS#	BL17	MA_CAS# [13:14]
SA_DM_0	AT45	MA_DM[7:0] [13]
SA_DM_1	BD44	
SA_DM_2	BD42	
SA_DM_3	AW38	
SA_DM_4	AW13	
SA_DM_5	BB38	
SA_DM_6	AV5	
SA_DM_7	AN6	
SA_DQS_0	AT46	MA_DQS[7:0] [13]
SA_DQS_1	BE48	
SA_DQS_2	BB43	
SA_DQS_3	BB37	
SA_DQS_4	BB16	
SA_DQS_5	BB16	
SA_DQS_6	BB2	
SA_DQS_7	AP3	
SA_DQS_8	AT47	MA_DQS[7:0] [13]
SA_DQS_9	BD47	
SA_DQS_10	BD41	
SA_DQS_11	BA37	
SA_DQS_12	BA16	
SA_DQS_13	BB17	
SA_DQS_14	BB1	
SA_DQS_15	AP2	
SA_MA_0	BL19	MA_A[13:0] [13:14]
SA_MA_1	BD20	
SA_MA_2	BD27	
SA_MA_3	BL24	
SA_MA_4	BL28	
SA_MA_5	BL27	
SA_MA_6	BL28	
SA_MA_7	BL28	
SA_MA_8	BA26	
SA_MA_9	BD19	
SA_MA_10	BE28	
SA_MA_11	BD30	
SA_MA_12	BL16	
SA_MA_13		
SA_RAS#	BE18	MA_RAS# [13:14]
SA_RCVEN#	AY20	
SA_WE#	BA19	MA_WE# [13:14]

[13] MB\_D[8:0]

## NU1E

MB D0	AP49	SB DQ 0
MB D1	AR51	SB DQ 1
MB D2	AM50	SB DQ 2
MB D3	AW51	SB DQ 3
MB D4	AN51	SB DQ 4
MB D5	AN50	SB DQ 5
MB D6	AV50	SB DQ 6
MB D7	BA50	SB DQ 7
MB D8	BA50	SB DQ 8
MB D9	BA50	SB DQ 9
MB D10	BA50	SB DQ 10
MB D11	BE50	SB DQ 11
MB D12	BA51	SB DQ 12
MB D13	AV49	SB DQ 13
MB D14	BF50	SB DQ 14
MB D15	BE49	SB DQ 15
MB D16	BB50	SB DQ 16
MB D17	BA44	SB DQ 17
MB D18	BA43	SB DQ 18
MB D19	BL43	SB DQ 19
MB D20	BB47	SB DQ 20
MB D21	BB43	SB DQ 21
MB D22	BB43	SB DQ 22
MB D23	BB42	SB DQ 23
MB D24	BB41	SB DQ 24
MB D25	BL41	SB DQ 25
MB D26	BL41	SB DQ 26
MB D27	BL41	SB DQ 27
MB D28	BB41	SB DQ 28
MB D29	BA40	SB DQ 29
MB D30	BL45	SB DQ 30
MB D31	BB37	SB DQ 31
MB D32	BB37	SB DQ 32
MB D33	BB37	SB DQ 33
MB D34	BB37	SB DQ 34
MB D35	BB37	SB DQ 35
MB D36	BB37	SB DQ 36
MB D37	BE12	SB DQ 37
MB D38	BE12	SB DQ 38
MB D39	BE12	SB DQ 39
MB D40	BE12	SB DQ 40
MB D41	BL5	SB DQ 41
MB D42	BB5	SB DQ 42
MB D43	BB5	SB DQ 43
MB D44	BB5	SB DQ 44
MB D45	BB5	SB DQ 45
MB D46	BB5	SB DQ 46
MB D47	BB5	SB DQ 47
MB D48	BE4	SB DQ 48
MB D49	BB1	SB DQ 49
MB D50	BB1	SB DQ 50
MB D51	BB1	SB DQ 51
MB D52	BB1	SB DQ 52
MB D53	BB1	SB DQ 53
MB D54	BB1	SB DQ 54
MB D55	BB1	SB DQ 55
MB D56	BB1	SB DQ 56
MB D57	BB1	SB DQ 57
MB D58	AB1	SB DQ 58
MB D59	AT2	SB DQ 59
MB D60	AT2	SB DQ 60
MB D61	AT2	SB DQ 61
MB D62	AT2	SB DQ 62
MB D63	AT2	SB DQ 63

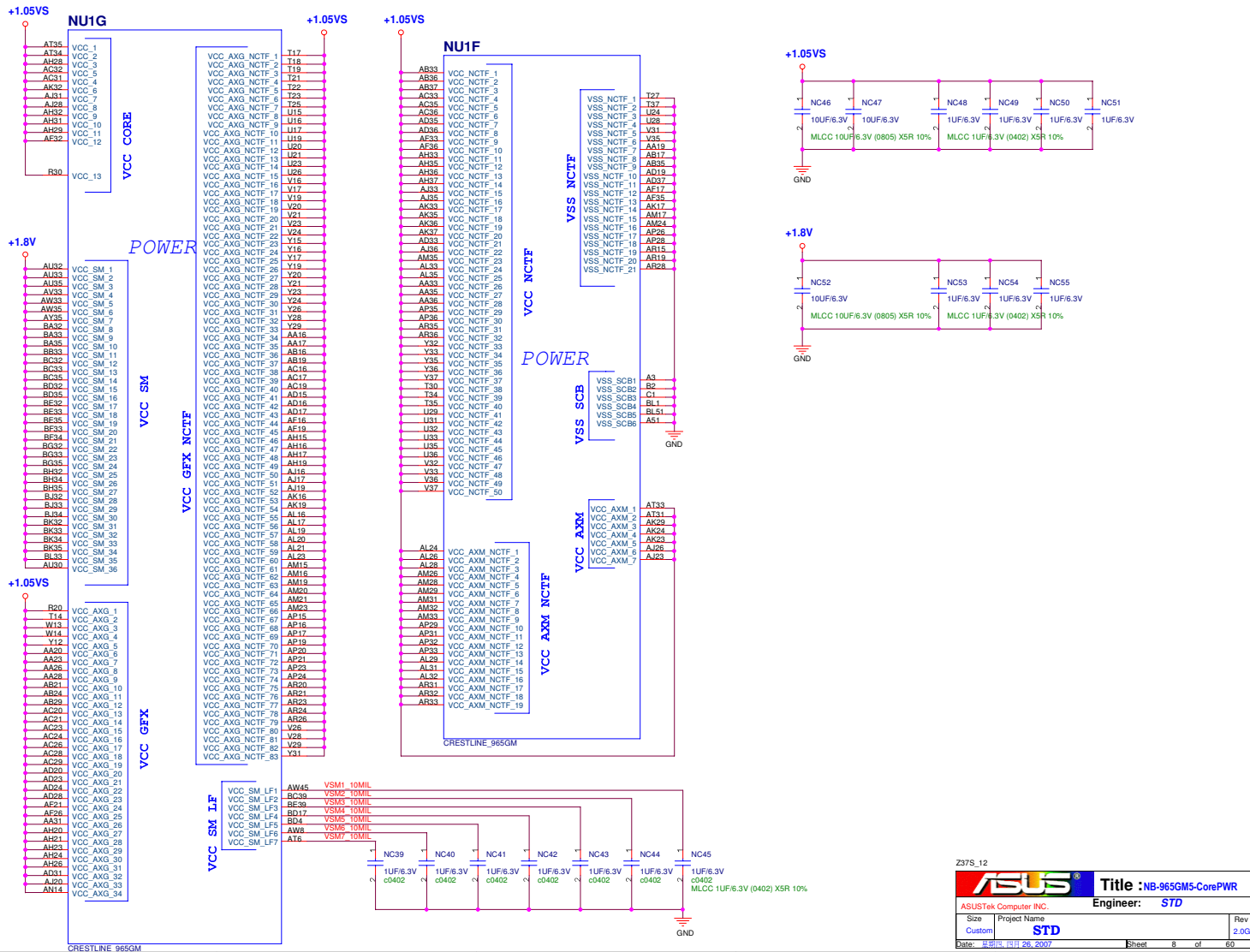
CRESTLINE\_965GM

DDR SYSTEM MEMORY B

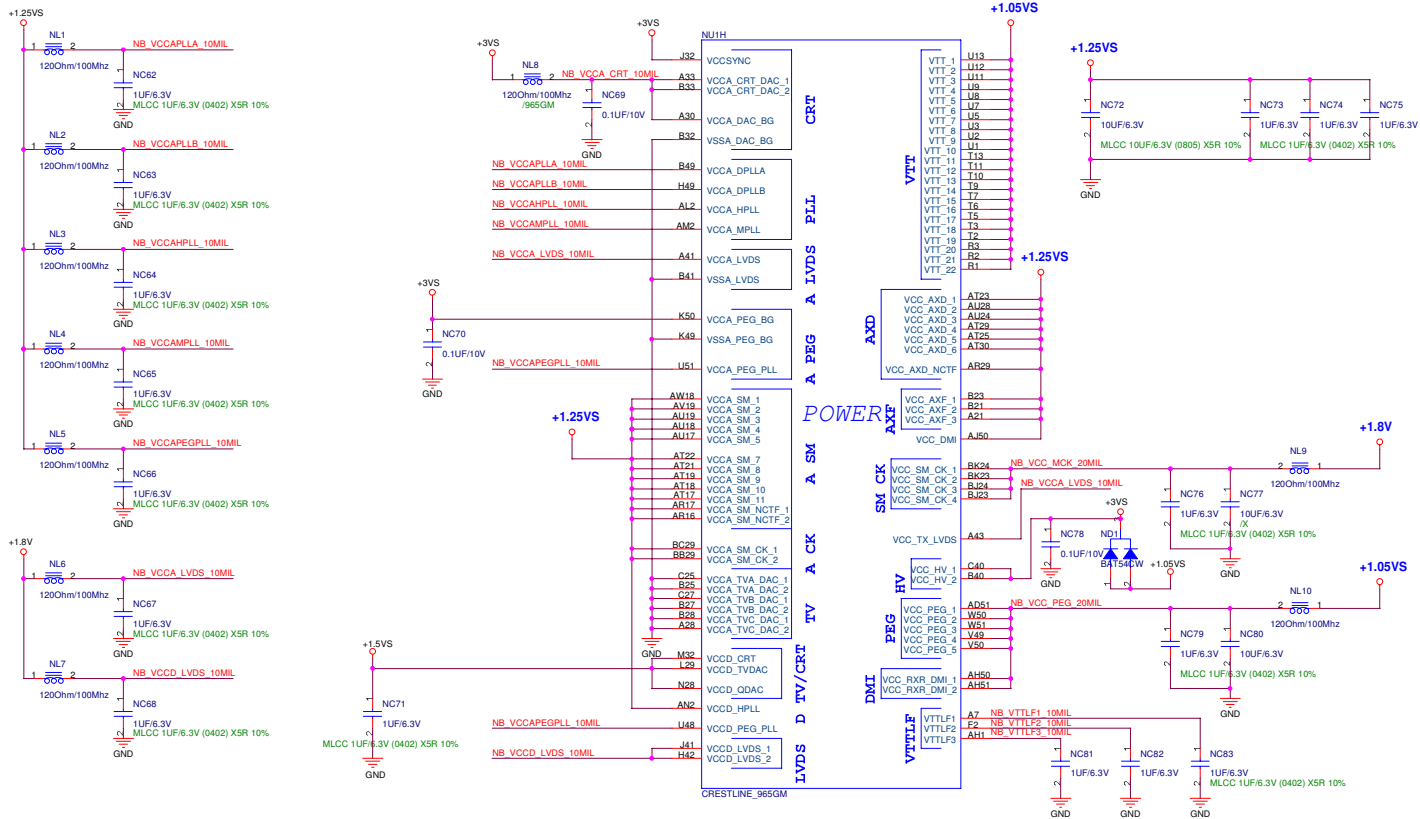
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SB BS_1	BG18	MB_BA1 [13:14]
SB BS_2	BB38	MB_BA2 [13:14]
SB_CAS#	BE17	MB_CAS# [13:14]
SB_DM_0	AR50	MB_DM[7:0] [13]
SB_DM_1	BD49	
SB_DM_2	BA45	
SB_DM_3	BA45	
SB_DM_4	BB15	
SB_DM_5	BB15	
SB_DM_6	BB15	
SB_DM_7	BB15	
SB_DQS_0	AT50	MB_DQS[7:0] [13]
SB_DQS_1	BD50	
SB_DQS_2	BB46	
SB_DQS_3	BB38	
SB_DQS_4	BB12	
SB_DQS_5	BB12	
SB_DQS_6	BB12	
SB_DQS_7	AV2	
SB_DQS_8	AU50	
SB_DQS_9	BB50	
SB_DQS_10	BB50	
SB_DQS_11	BB50	
SB_DQS_12	BB50	
SB_DQS_13	BB50	
SB_DQS_14	BB50	
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SB_DQS_17	BB50	
SB_DQS_18	BB50	
SB_DQS_19	BB50	
SB_DQS_20	BB50	
SB_DQS_21	BB50	
SB_DQS_22	BB50	
SB_DQS_23	BB50	
SB_DQS_24	BB50	
SB_DQS_25	BB50	
SB_DQS_26	BB50	
SB_DQS_27	BB50	
SB_DQS_28	BB50	
SB_DQS_29	BB50	
SB_DQS_30	BB50	
SB_DQS_31	BB50	
SB_DQS_32	BB50	
SB_DQS_33	BB50	
SB_DQS_34	BB50	
SB_DQS_35	BB50	
SB_DQS_36	BB50	
SB_DQS_37	BB50	
SB_DQS_38	BB50	
SB_DQS_39	BB50	
SB_DQS_40	BB50	
SB_DQS_41	BB50	
SB_DQS_42	BB50	
SB_DQS_43	BB50	
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SB_DQS_46	BB50	
SB_DQS_47	BB50	
SB_DQS_48	BB50	
SB_DQS_49	BB50	
SB_DQS_50	BB50	
SB_DQS_51	BB50	
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SB_DQS_59	BB50	
SB_DQS_60	BB50	
SB_DQS_61	BB50	
SB_DQS_62	BB50	
SB_DQS_63	BB50	

Z378\_12









Z37S\_12

		Title : NB-965GM6-IOPWR	
ASUSTek Computer INC.		Engineer: STD	
Size Custom	Project Name STD	Rev 2.0G	
Date: 星期日, 四月 26, 2007		Sheet 9 of 60	



# NU1I

A13	VSS 1	VSS 100
A15	VSS 2	AW26
A17	VSS 3	D13
A24	VSS 4	AW32
AA24	VSS 5	AW5
VSS 6	VSS 105	D3
AA29	VSS 7	D32
AB20	VSS 8	D39
AB23	VSS 9	DA5
AB26	VSS 10	AY37
AB28	VSS 11	AY42
AB31	VSS 12	AY43
AC10	VSS 13	AY45
AC13	VSS 14	AY47
AC3	VSS 15	AY50
AC39	VSS 16	B10
AC43	VSS 17	B20
AC47	VSS 18	B24
AD1	VSS 19	B29
AD21	VSS 20	B30
AD26	VSS 21	B38
AD28	VSS 22	B43
AD3	VSS 23	B46
AD41	VSS 24	B5
AD45	VSS 25	B8
AD49	VSS 26	BA1
AD5	VSS 27	BA17
AD50	VSS 28	BA19
AD6	VSS 29	BA2
AE10	VSS 30	BA24
AE14	VSS 31	BB12
AE6	VSS 32	BB25
AF20	VSS 33	BB40
AF23	VSS 34	BB44
AF24	VSS 35	BB49
AF31	VSS 36	BB8
AG2	VSS 37	BC16
AG38	VSS 38	BC24
AG43	VSS 39	BC25
AG50	VSS 40	BC36
AH3	VSS 41	BC40
AH40	VSS 42	BC51
AH41	VSS 43	BD13
AH44	VSS 44	BD2
AH7	VSS 45	BD28
AH9	VSS 46	BD45
AJ11	VSS 47	BD48
AJ13	VSS 48	BD5
AJ21	VSS 49	BE1
AJ24	VSS 50	BE19
AJ29	VSS 51	BE23
AJ3	VSS 52	BE30
AJ45	VSS 53	BE42
AJ49	VSS 54	BE5
AK20	VSS 55	BE16
AK21	VSS 56	L33
AK26	VSS 57	BF16
AK28	VSS 58	L49
AK31	VSS 59	BF36
AK51	VSS 60	BQ19
AL1	VSS 61	BQ2
AM11	VSS 62	BQ24
AM13	VSS 63	BQ29
AM3	VSS 64	BQ39
AM4	VSS 65	BQ48
AM41	VSS 66	BQ5
AM45	VSS 67	BQ51
AN1	VSS 68	BH17
AN38	VSS 69	BH20
AN39	VSS 70	BH44
AN43	VSS 71	BH46
AN5	VSS 72	BH5
AN7	VSS 73	BH11
AP4	VSS 74	BJ13
AP48	VSS 75	BJ38
AP50	VSS 76	B4
AP51	VSS 77	B42
AR2	VSS 78	B46
AR29	VSS 79	BK15
AR44	VSS 80	BK17
AR7	VSS 81	BK25
AT10	VSS 82	BK29
AT14	VSS 83	BK36
AT49	VSS 84	BK40
AU1	VSS 85	BK44
AU23	VSS 86	BK6
AU29	VSS 87	BK8
AU3	VSS 88	BL11
AU36	VSS 89	BL13
AU49	VSS 90	BL19
AU51	VSS 91	BL22
AV39	VSS 92	BL27
AW1	VSS 93	BL47
AW12	VSS 94	C12
AW16	VSS 95	C16
	VSS 96	C19
	VSS 97	C28
	VSS 98	C29
	VSS 99	C33
		C36
		C41

CRESTLINE\_965GM



# NU1J

C46	VSS 199	VSS 287
C50	VSS 200	VSS 288
C7	VSS 201	VSS 289
D13	VSS 202	VSS 290
D24	VSS 203	VSS 291
D3	VSS 204	VSS 292
D32	VSS 205	VSS 293
D39	VSS 206	VSS 294
DA5	VSS 207	VSS 295
AY37	VSS 208	VSS 296
AY42	VSS 209	VSS 297
AY43	VSS 210	VSS 298
AY45	VSS 211	VSS 299
AY47	VSS 212	VSS 300
AY50	VSS 213	VSS 301
B10	VSS 214	VSS 302
B20	VSS 215	VSS 303
B24	VSS 216	VSS 304
B29	VSS 217	VSS 305
B30	VSS 218	
B38	VSS 219	
B43	VSS 220	
B46	VSS 221	
B5	VSS 222	VSS 306
B8	VSS 223	VSS 307
BA1	VSS 224	VSS 308
BA17	VSS 225	VSS 309
BA19	VSS 226	VSS 310
BA2	VSS 227	VSS 311
BA24	VSS 228	VSS 312
BB12	VSS 229	VSS 313
BB25	VSS 230	
BB40	VSS 231	
BB44	VSS 232	
BB49	VSS 233	
BB8	VSS 234	
BC16	VSS 235	
BC24	VSS 236	
BC25	VSS 237	
BC36	VSS 238	
BC40	VSS 239	
BC51	VSS 240	
BD13	VSS 241	
BD2	VSS 242	
BD28	VSS 243	
BD45	VSS 245	
BD48	VSS 246	
BD5	VSS 247	
BE1	VSS 248	
BE19	VSS 249	
BE23	VSS 250	
BE30	VSS 251	
BE42	VSS 252	
BE5	VSS 253	
BE16	VSS 254	
L33	VSS 255	
BF16	VSS 256	
L49	VSS 257	
BF36	VSS 258	
BQ19	VSS 259	
BQ2	VSS 260	
BQ24	VSS 261	
BQ29	VSS 262	
BQ39	VSS 263	
BQ48	VSS 264	
BQ5	VSS 265	
BQ51	VSS 266	
BH17	VSS 267	
BH20	VSS 268	
BH44	VSS 269	
BH46	VSS 270	
BH5	VSS 271	
BH11	VSS 272	
BJ13	VSS 273	
BJ38	VSS 274	
B4	VSS 275	
B42	VSS 276	
B46	VSS 277	
BK15	VSS 278	
BK17	VSS 279	
BK25	VSS 280	
BK29	VSS 281	
BK36	VSS 282	
BK40	VSS 283	
BK44	VSS 284	
BK6	VSS 285	
BK8	VSS 286	
BL11	VSS 287	
BL13	VSS 288	
BL19	VSS 289	
BL22	VSS 290	
BL27	VSS 291	
BL47	VSS 292	
C12	VSS 293	
C16	VSS 294	
C19	VSS 295	
C28	VSS 296	
C29	VSS 297	
C33	VSS 298	
C36	VSS 299	
C41	VSS 300	

CRESTLINE\_965GM



VSS

W11	VSS 287
W39	VSS 288
W43	VSS 289
W47	VSS 290
W5	VSS 291
W7	VSS 292
Y19	VSS 293
Y2	VSS 294
Y41	VSS 295
Y45	VSS 296
Y49	VSS 297
Y5	VSS 298
Y50	VSS 299
Y11	VSS 300
Y25	VSS 301
Y29	VSS 302
Y31	VSS 303
Y33	VSS 304
Y35	VSS 305
Y37	VSS 306
Y39	VSS 307
Y41	VSS 308
Y43	VSS 309
Y45	VSS 310
Y47	VSS 311
Y49	VSS 312
Y51	VSS 313



GND

Z37S\_12

		<b>Title :</b> NB-965GM7-GND	
ASUSTek Computer INC.		<b>Engineer:</b> STD	
Size Custom	Project Name <b>STD</b>	Rev 2.00	
Date: 2008.03.28.2007		Sheet 10 of 60	

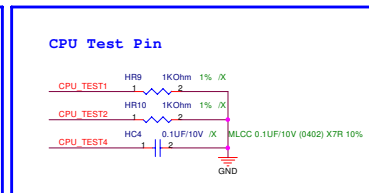




## SOCKETPE



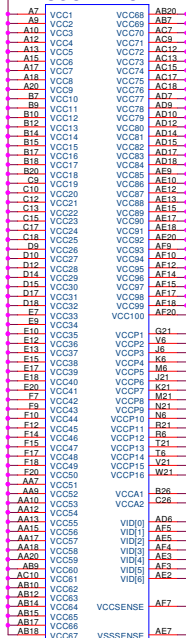
Comp0,2 connect with  $Z_0=27.4 \text{ ohm}$ ,  
make trace length shorter than  $0.5''$ .  
Comp 1,3 connect with  $Z_0=55 \text{ ohm}$ ,  
make trace length shorter than  $0.5''$ .



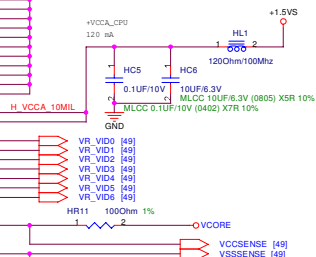


## VCORE

## SOCKETPC

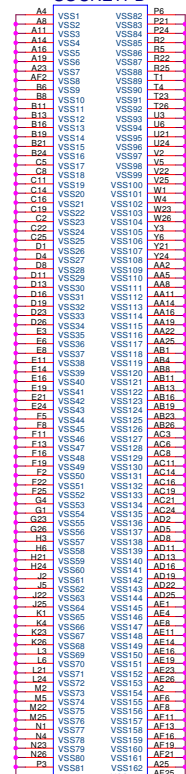


+1.05VS

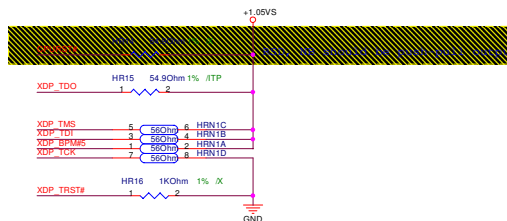
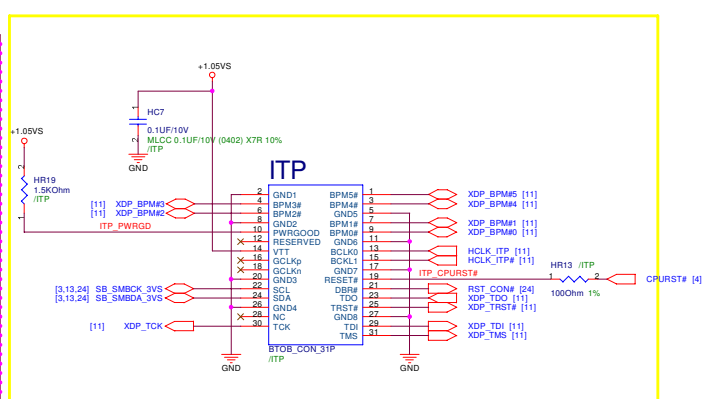


VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of GPI

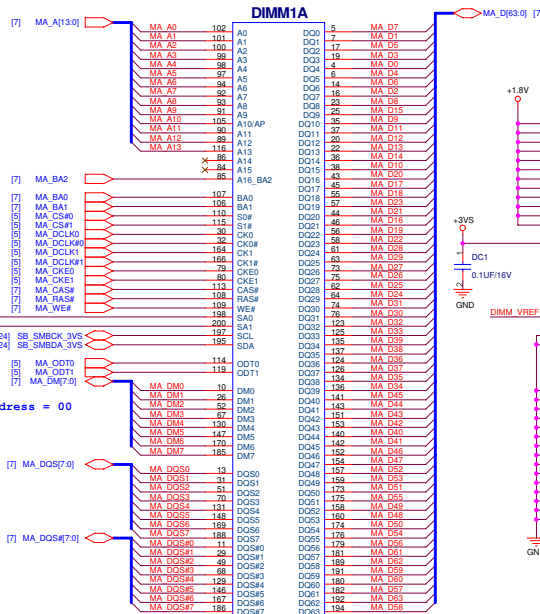
## SOCKETP



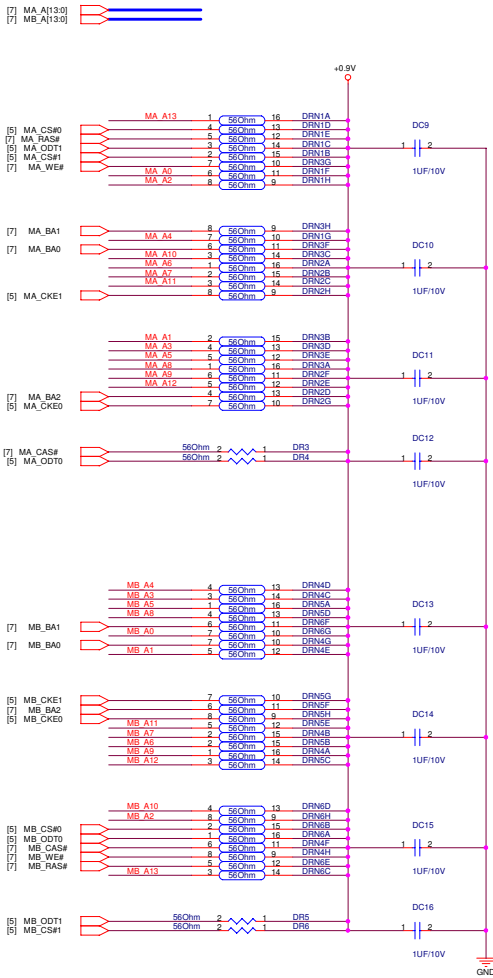
## SOCKET478B





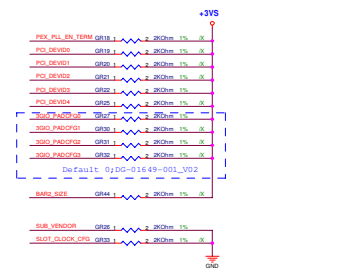
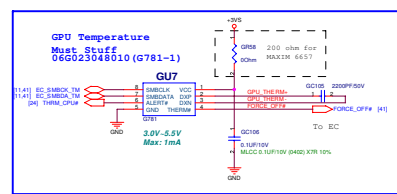
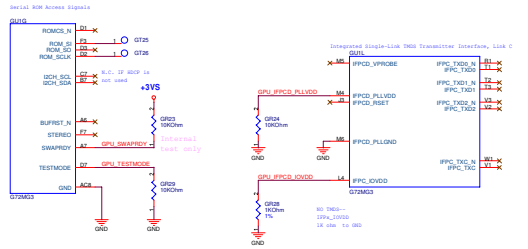
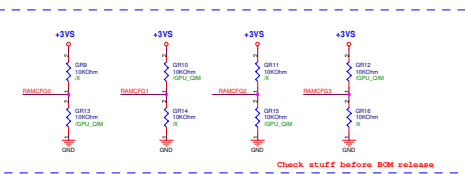
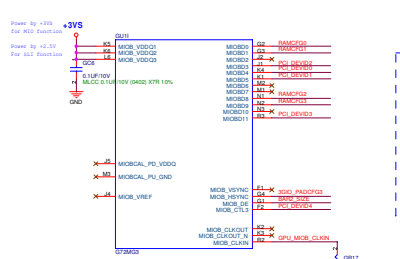
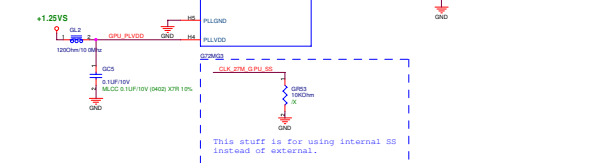
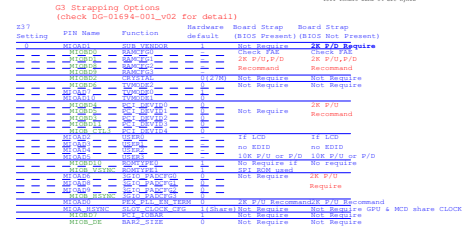
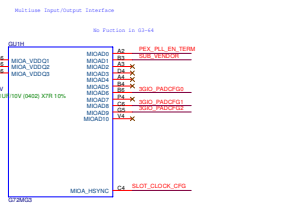
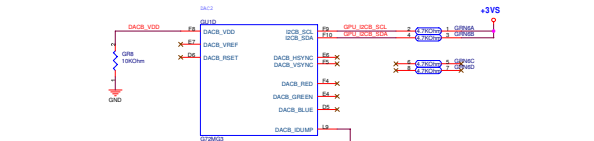
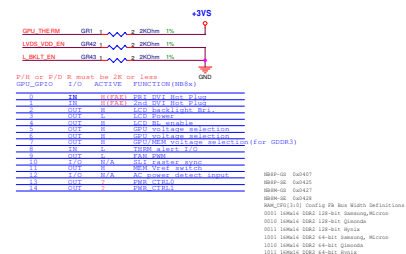
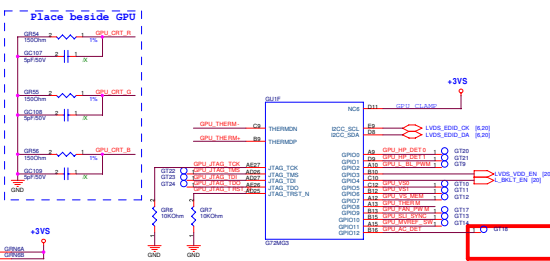
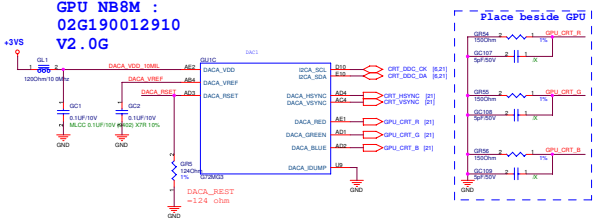








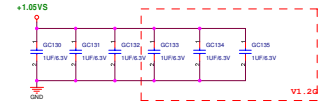
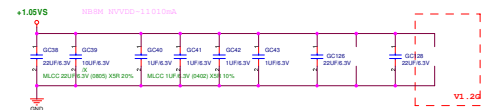
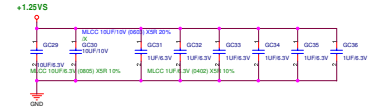
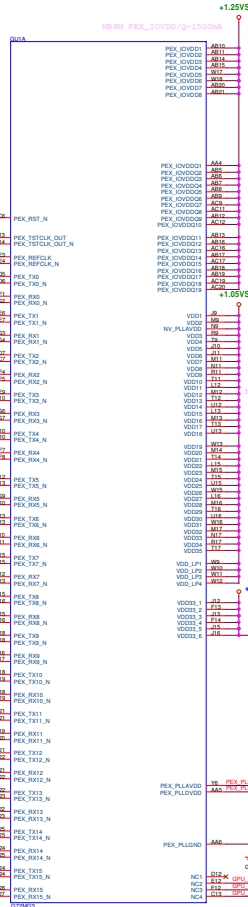
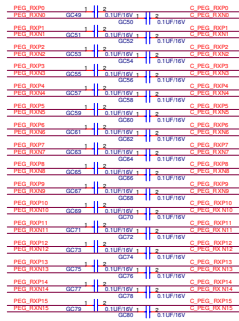
```
GPU NB8M :
02G190012910
V2.0G
```











PEX\_R0010 - 1.000000

PEX\_R0011 - 1.000000

PEX\_R0012 - 1.000000

PEX\_R0013 - 1.000000

PEX\_R0014 - 1.000000

PEX\_R0015 - 1.000000

PEX\_R0016 - 1.000000

PEX\_R0017 - 1.000000

PEX\_R0018 - 1.000000

PEX\_R0019 - 1.000000

PEX\_R0020 - 1.000000

PEX\_R0021 - 1.000000

PEX\_R0022 - 1.000000

PEX\_R0023 - 1.000000

PEX\_R0024 - 1.000000

PEX\_R0025 - 1.000000

PEX\_R0026 - 1.000000

PEX\_R0027 - 1.000000

PEX\_R0028 - 1.000000

PEX\_R0029 - 1.000000

PEX\_R0030 - 1.000000

PEX\_R0031 - 1.000000

PEX\_R0032 - 1.000000

PEX\_R0033 - 1.000000

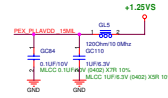
PEX\_R0034 - 1.000000

PEX\_R0035 - 1.000000

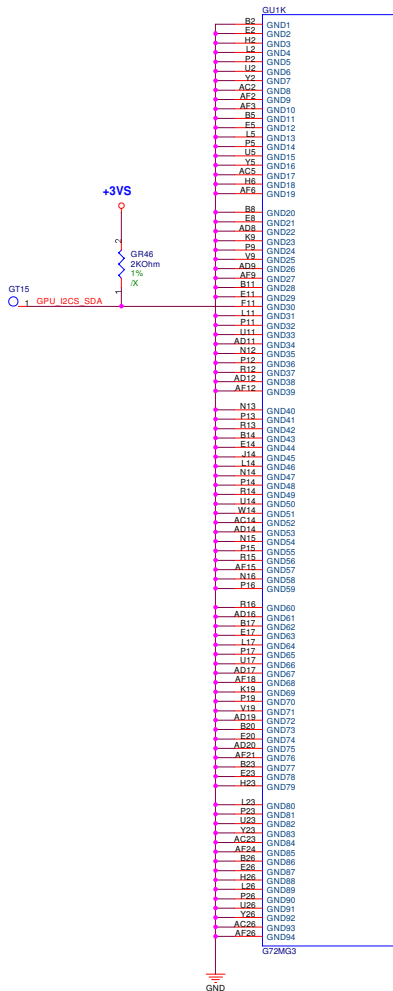
PEX\_R0036 - 1.000000

PEX\_R0037 - 1.000000

PEX\_R0038 - 1.000000

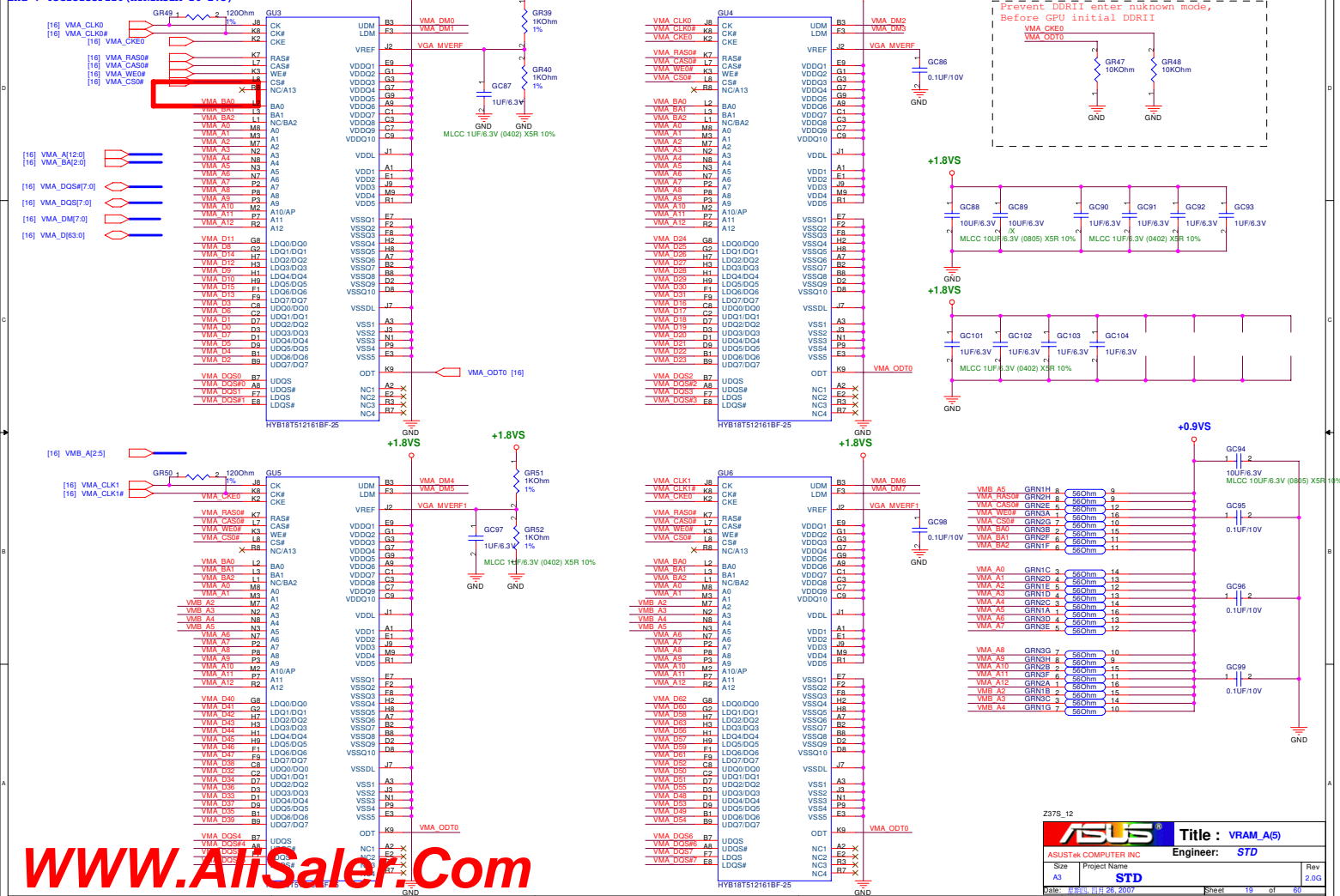






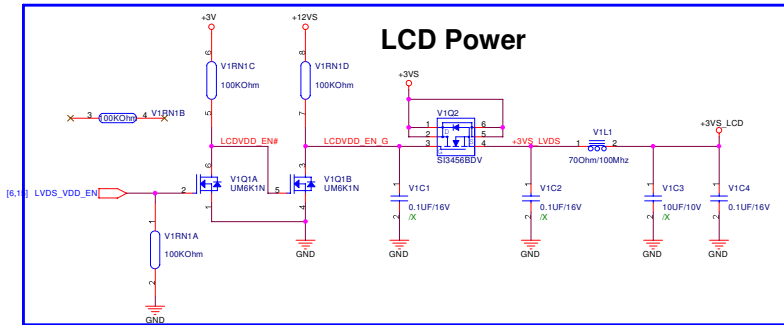


```
VRAM CHIP:
1st : 03G15133F010 (INFINEON32M*16-2.5)
2nd : 03G15133F110 (HYNIX32M*16-2.5)
```

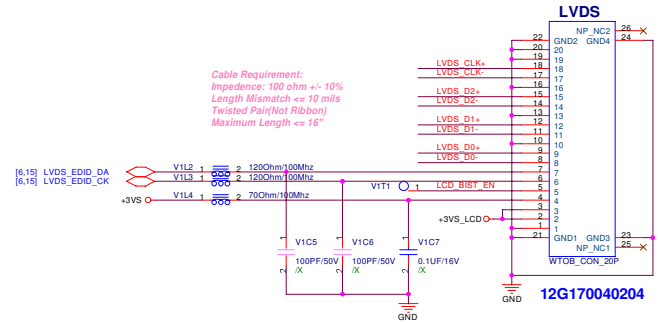




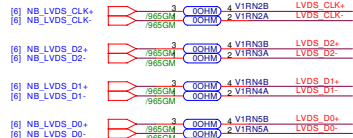
## LCD Power



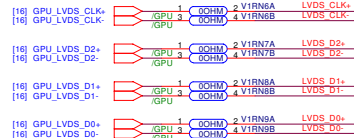
## LCD LVDS Connector



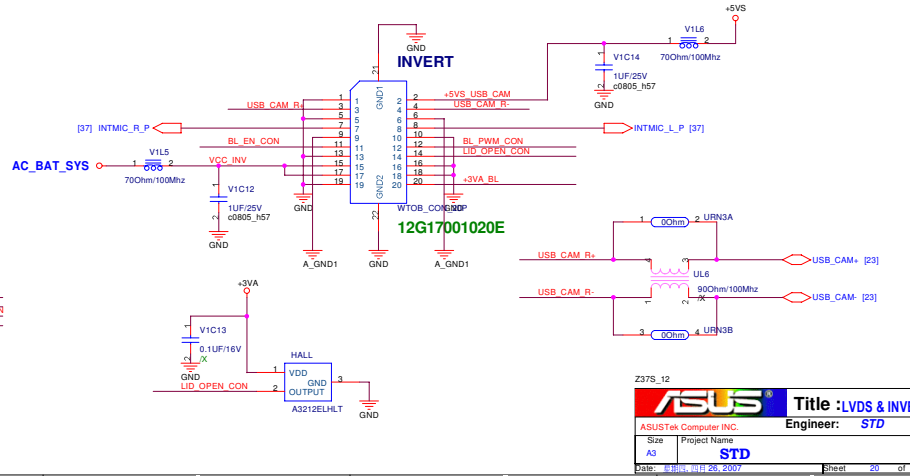
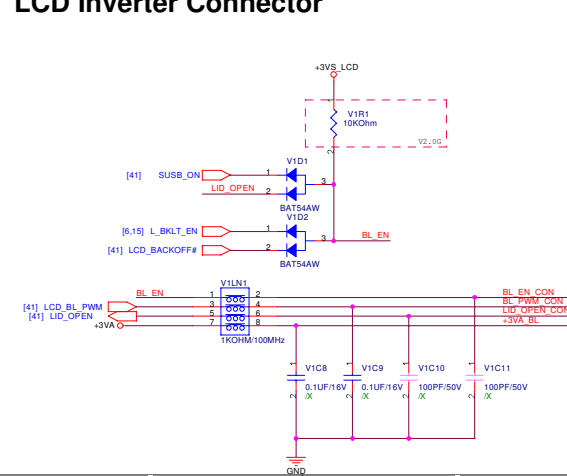
### LVDS from 965GM



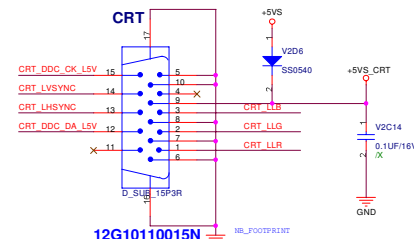
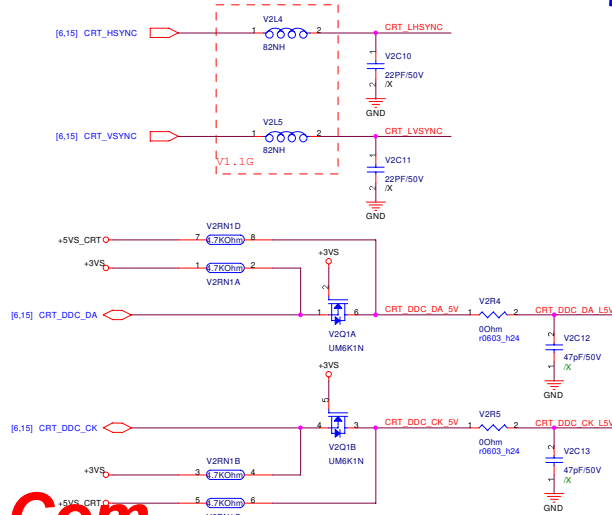
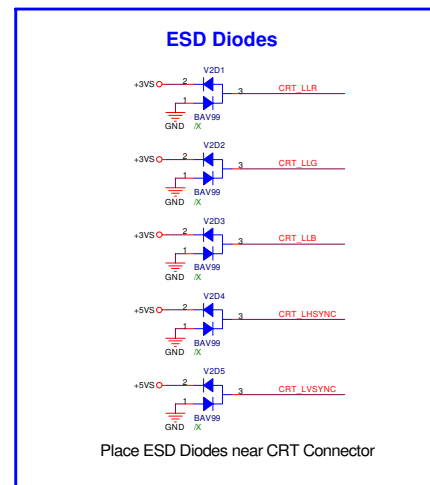
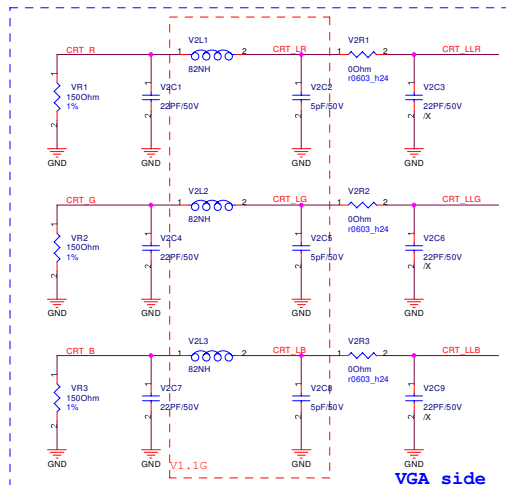
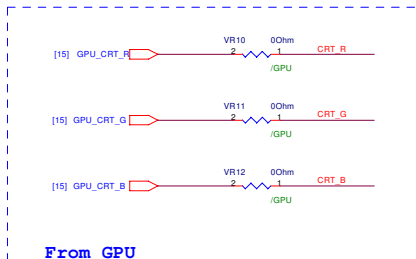
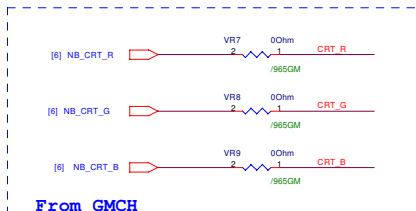
### LVDS from GPU-NB8M



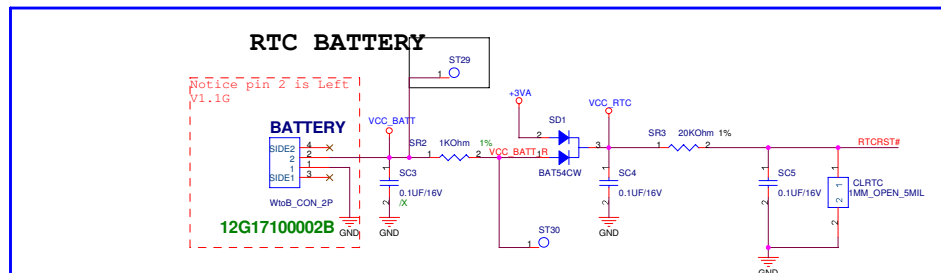
## LCD Inverter Connector











Pin connections for the 74VHC04 hex inverters:

- SB\_INTRUDER#** (red) to pin 3, connected to **1MΩ** and **4 SRN1B** (blue).
- SB\_INTRVNT#** (red) to pin 5, connected to **1MΩ** and **4 SRN1C** (blue).
- SB\_INTRVENC#** (red) to pin 7, connected to **1MΩ** and **4 SRN1D** (blue).
- A2OGATE** (red) to pin 10, connected to **10kΩ** and **4 SRN2D** (blue).
- RBRST#** (red) to pin 5, connected to **10kΩ** and **4 SRN2C** (blue).
- H\_FERR#** (red) to pin 1, connected to **560Ω** and **4 SRN3A** (blue).
- H\_THRMTRIP#** (red) to pin 3, connected to **560Ω** and **4 SRN3B** (blue).
- H\_FERR#** (red) to pin 5, connected to **560Ω** and **4 SRN3C** (blue).
- H\_THRMTRIP#** (red) to pin 7, connected to **560Ω** and **4 SRN3D** (blue).
- IDE\_PIOROY** (red) to pin 1, connected to **4.7kΩ** and **4 SRN4A** (blue).
- IDE\_PIOROY** (red) to pin 3, connected to **4.7kΩ** and **4 SRN4B** (blue).
- IDE\_PIOROY** (red) to pin 5, connected to **4.7kΩ** and **4 SRN4C** (blue).
- IDE\_PIOROY** (red) to pin 7, connected to **4.7kΩ** and **4 SRN4D** (blue).

Power supply connections:

- VCC, RTN** (red) to pin 14.
- +3VS** (red) to pin 13.
- +1.65VS** (red) to pin 12.
- ID** (red) to pin 11.

```
[3] CLK_SATA_SB#
[3] CLK_SATA_SB
```

ASUSTek Computer INC.		Engineer: STD	
Size Custom	Project Name STD	Rev 2.2G	
Date: 星期四, 四月 26, 2007		Sheet 22 of 60	







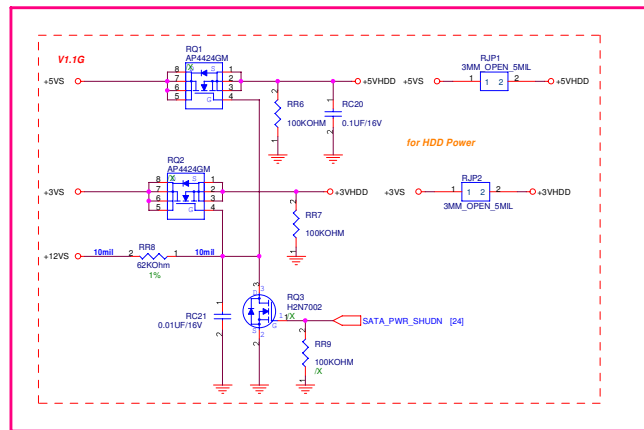
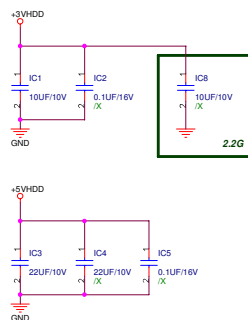
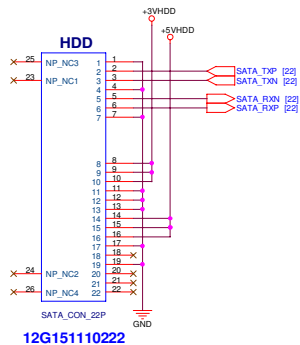




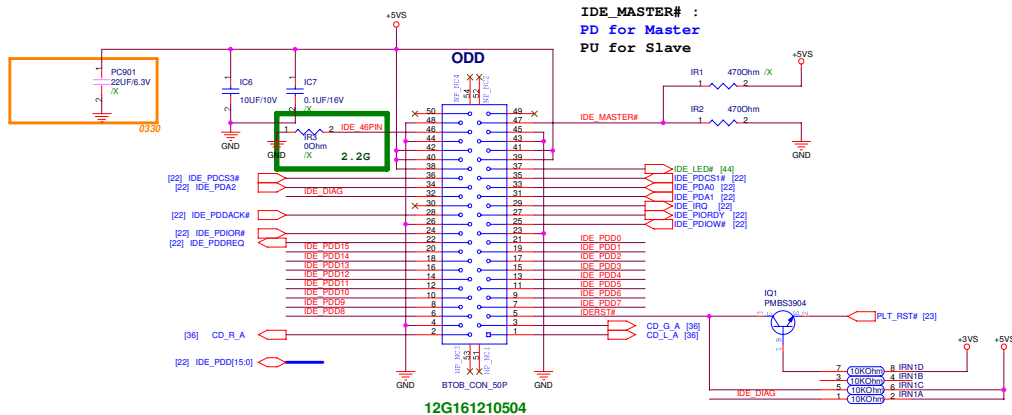




**SATA HDD**

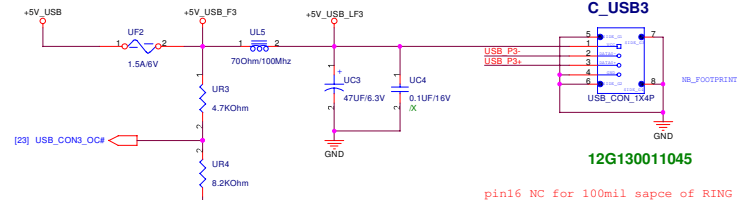
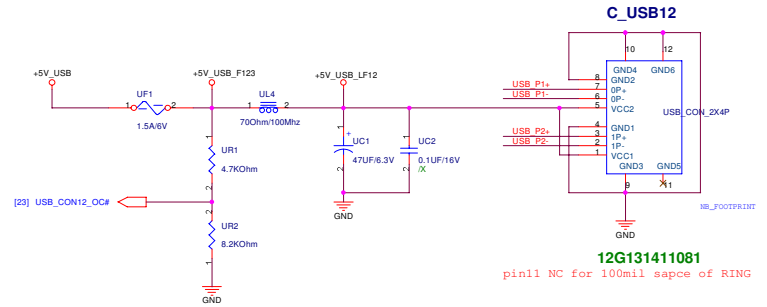
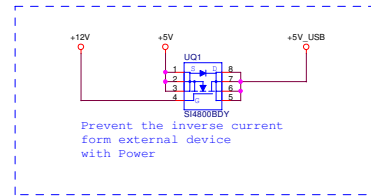
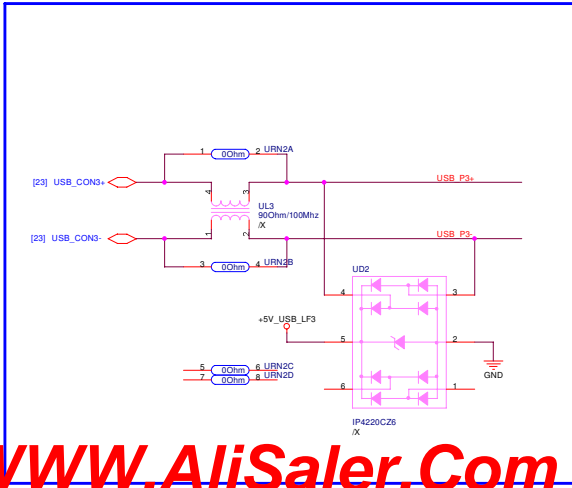
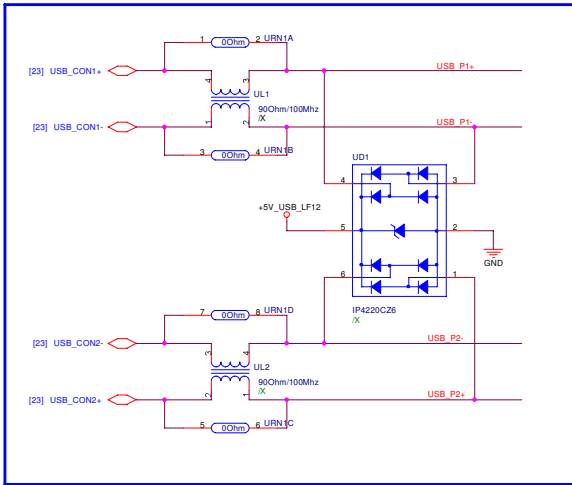


**ODD**





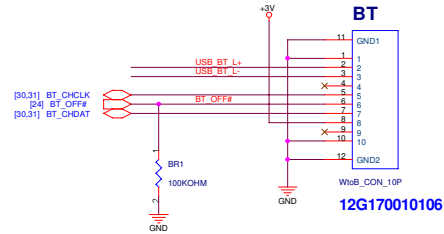
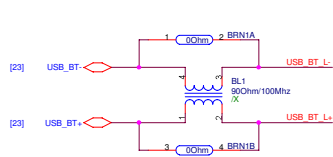
## All close to USB connectors



WWW.AliSaler.Com



# Bluetooth Connector

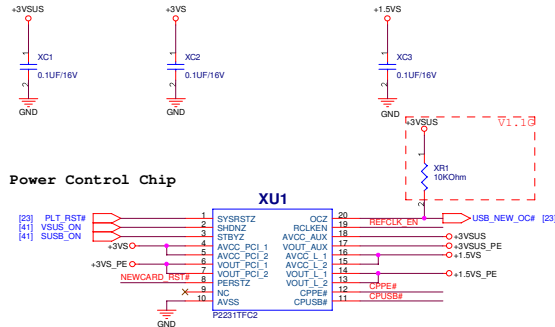


BT\_OFF# : (connect to GPO, push-pull, default High)  
 0 => BT Disabled  
 1 => BT Enabled

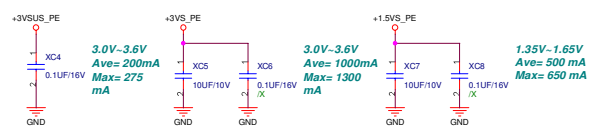
Z37S\_12



## Decouple Cap. (Near XU1)

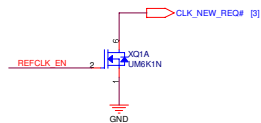


## Decouple Cap. (Near Express connector)

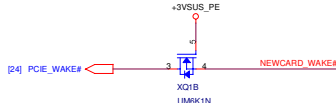


12G161300261

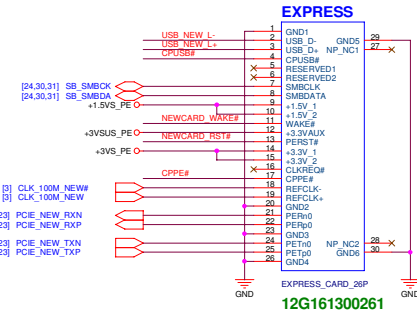
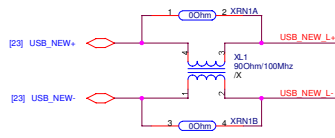
## NEWCARD CLK Request



## NEWCARD Wake#



## USB CHOKE FOR EMI

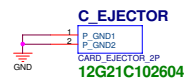


EXPRESS\_CARD\_26P

12G161300261

!! ExpressCard Standard 1.0:  
Change Pin7 from RESERVED to SMBCLK  
Change Pin8 from SMBCLK to SMBDATA  
Change Pin9 from SMBDATA to +1.5V

## NewCard Ejector



C\_EJECTOR

12G21C102604

Z37S\_12

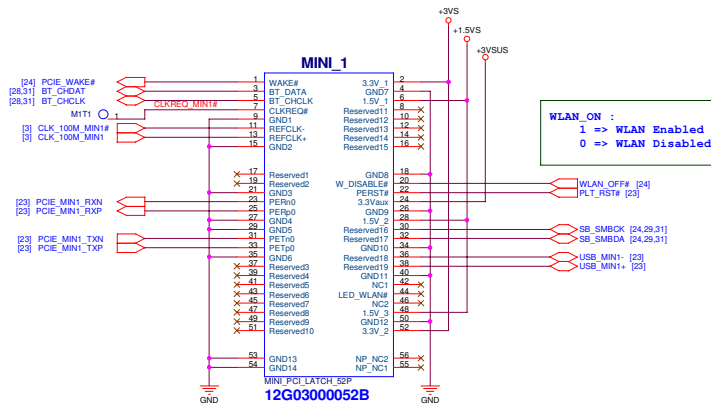
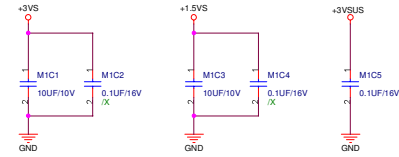


# Decouple Cap. (Near C\_MINICARD1)

+3.003V~+3.597V  
Max= 750 mA

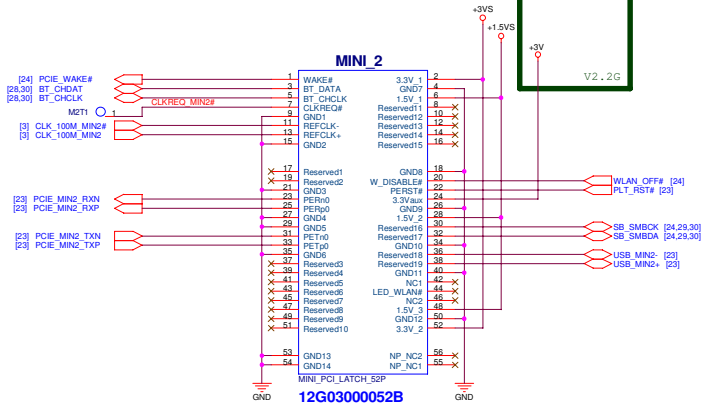
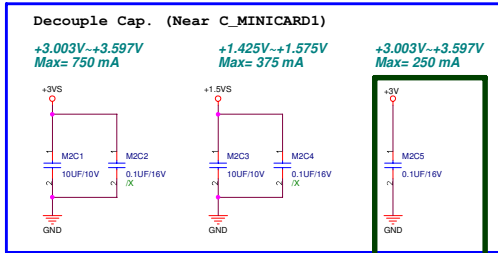
+1.425V~+1.575V  
Max= 375 mA

+3.003V~+3.597V  
Max= 250 mA



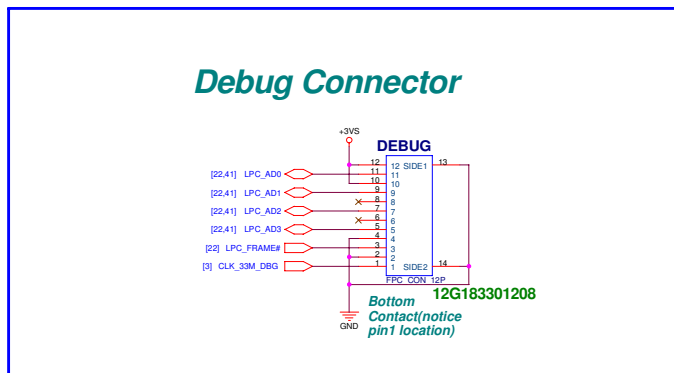
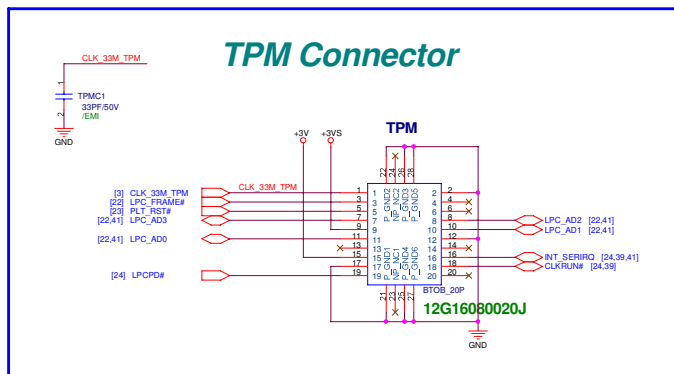
Z375\_12





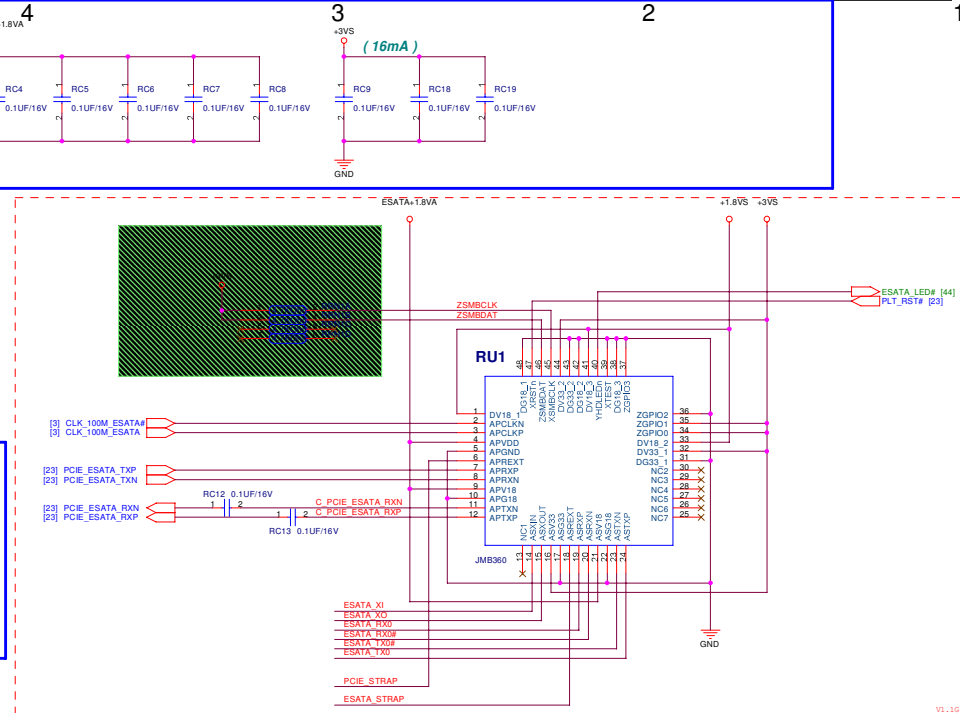
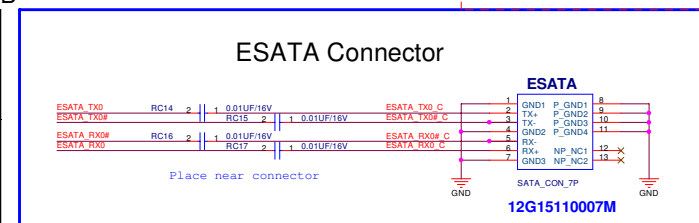
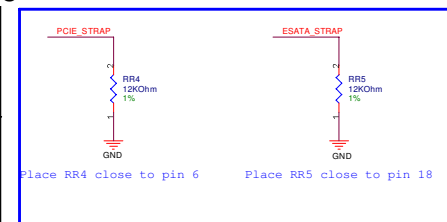
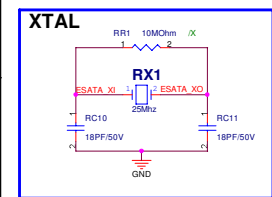
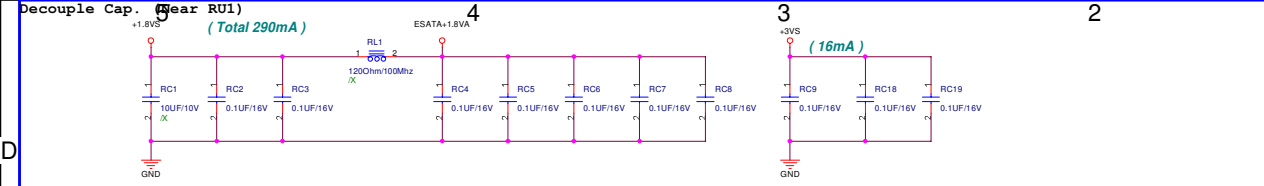
Z375\_12





Z37S\_12



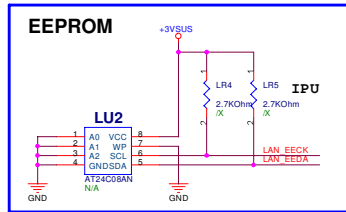
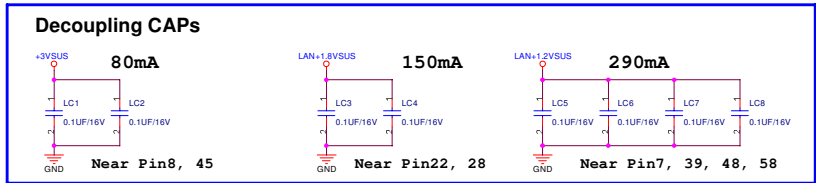




### PCIE X1 Interface

The diagram illustrates the PCIE X1 Interface with the following components:

- Signal Lines:**
  - PCIE\_LAN\_RXN** (Red arrow pointing left)
  - PCIE\_LAN\_RXP** (Red arrow pointing left)
  - PCIE\_LAN\_TXN** (Red arrow pointing right)
  - PCIE\_LAN\_TXP** (Red arrow pointing right)
- Voltage Levels:**
  - LC15** (0.1UF/16V) connected to **PCIE\_LAN\_RXN**
  - LC16** (0.1UF/16V) connected to **PCIE\_LAN\_RXP**
- Labels:**
  - C PCIE LAN\_RXN** (Red text)
  - C PCIE LAN\_RXP** (Red text)




## Differential Termination

The diagram illustrates a differential termination circuit for four signal lines. A common ground is connected to the bottom of four capacitors (1000PF/50V). The top of each capacitor is connected to a signal line. Each signal line has a series resistor (LRB, LRT, LRB, LRT, LRB, LRT, LRB, LRT) and a 2 ohm termination resistor to ground. The signal lines are labeled LMDI\_A+, LMDI\_A-, LMDI\_B+, LMDI\_B-, LMDI\_C+, LMDI\_C-, LMDI\_D+, and LMDI\_D-.

## Compensation

A circuit diagram showing a compensation network. A red line labeled `LAN_RSET` is connected to a blue resistor labeled `LR1`. The resistor has a value of `4.99KOhm` and a tolerance of `1%`. The other end of the resistor is connected to a red ground symbol labeled `GND`.

# LOM Enabled



The diagram shows a circuit for enabling LOM. A red wire labeled '+3VSUS' is connected to the top terminal of a resistor labeled 'LR3' with a value of '2.7KOhm'. The bottom terminal of the resistor is connected to a red wire labeled 'LOM\_EN'.

Pin	MDI			MDIX		
	1000BASE-T	1000BASE-TX	10BASE-T	1000BASE-T	1000BASE-TX	10BASE-T
MDI(Pin1)	BL_Ctx	TX <sub>1</sub>	TX <sub>1</sub>	BL_Ctx	TX <sub>1</sub>	TX <sub>1</sub>
MDI(Pin2)	BL_Ctx	TX <sub>2</sub>	TX <sub>2</sub>	BL_Ctx	TX <sub>2</sub>	TX <sub>2</sub>
MDI(Pin3)	BL_Ctx	unused	unused	BL_Ctx	unused	unused
MDI(Pin4)	BL_Ctx	unused	unused	BL_Ctx	unused	unused



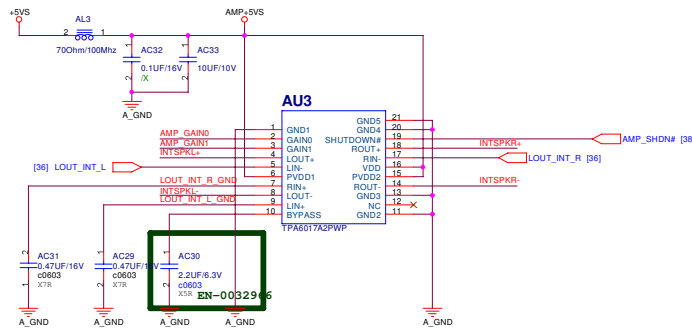




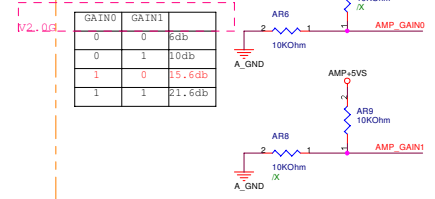




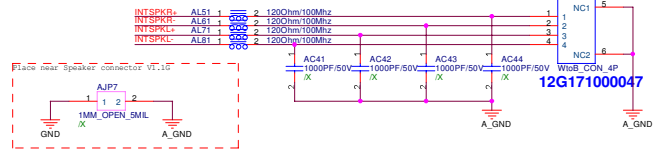
## Audio Amp.



## GAIN Control



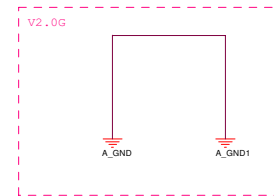
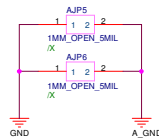
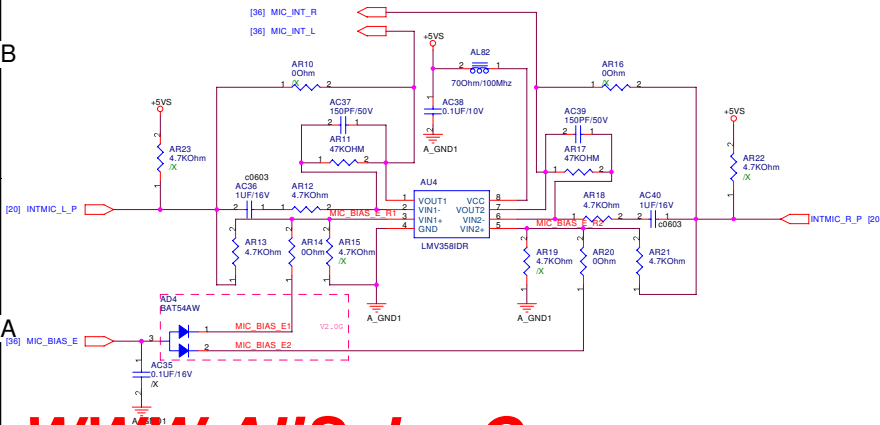
## SPEAKER



## Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz

Place Near INTMIC Connector



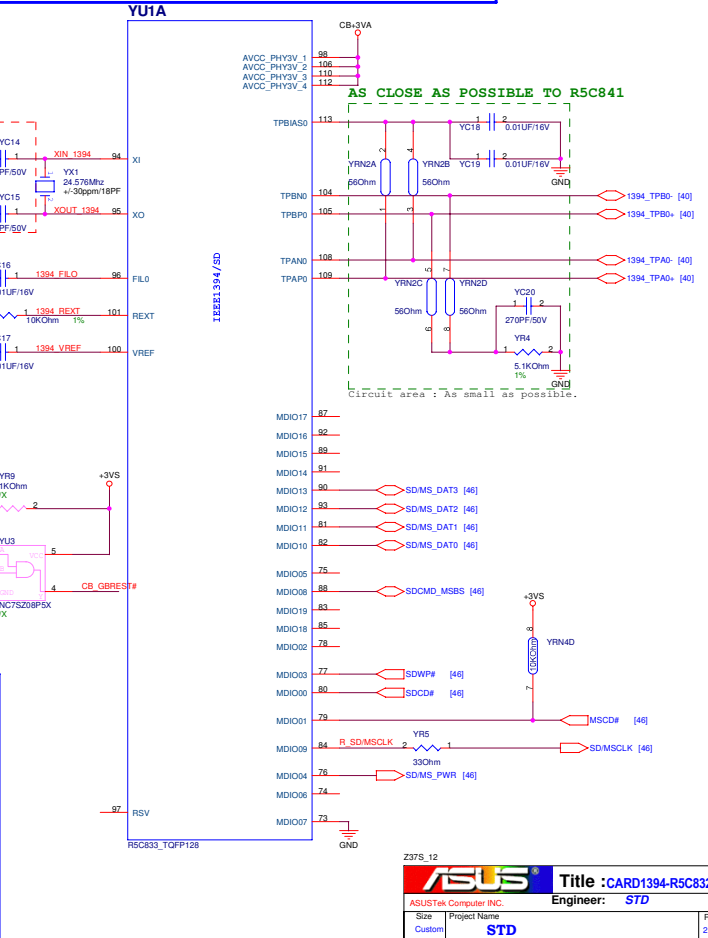
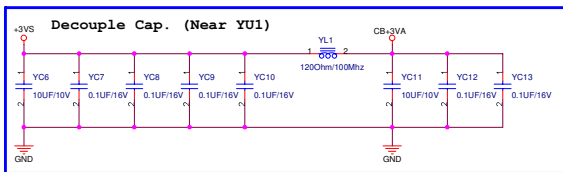
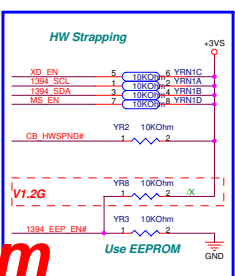
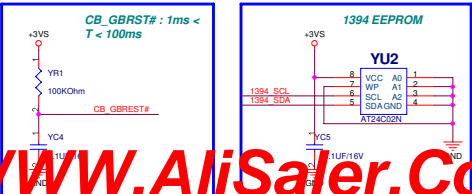
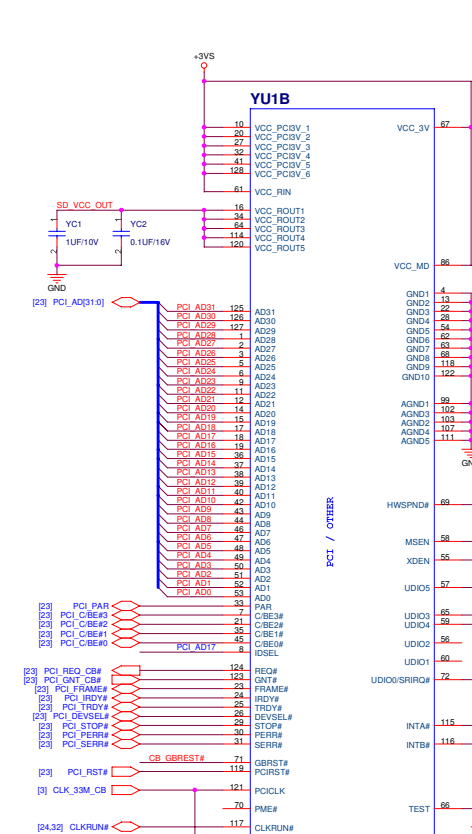
Z37S\_12

<b>ASUS</b>		Title : Audio 2	
ASUSTek Computer INC.		Engineer: STD	
Size	Project Name	Rev	
A3	STD	2.00	
Date: 11/03/2007	Sheet	37	of 60

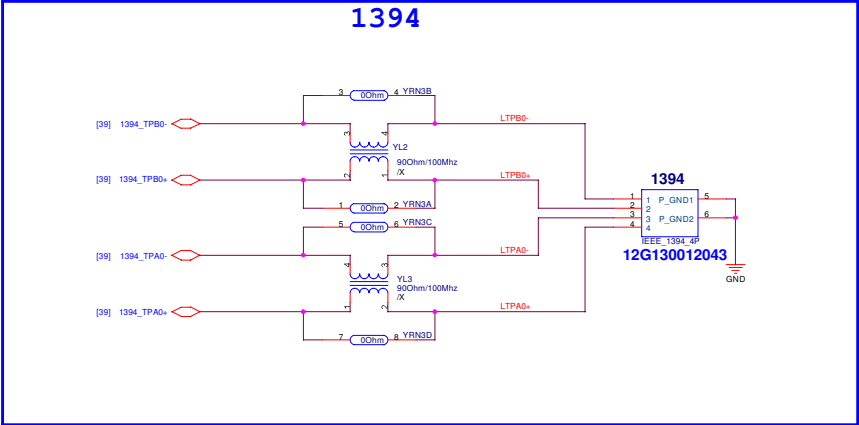












Z375\_12







ISA ROM

EC Hardware Strapping

[ FA3/ BADDR1 : FA2/ BADDR0 ]

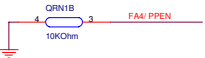
00: PNPCNG Access Register Pair Are 002Eh and 002Fh  
01: PNPCNG Access Register Pair Are 004Eh and 004Fh  
10: PNPCNG Access Register Pair Are Determined by  
EC Domain Registers SWCBALR and SWCBAHR.  
11: Reserved



Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal  
1: KBS Interface Pins Are Switched to Parallel Port  
Interface for In-System Programming

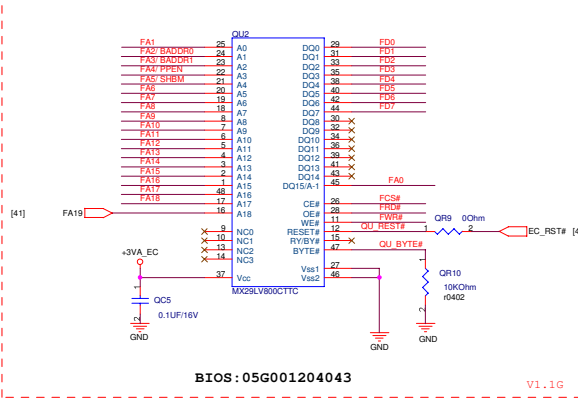
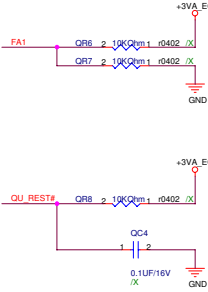
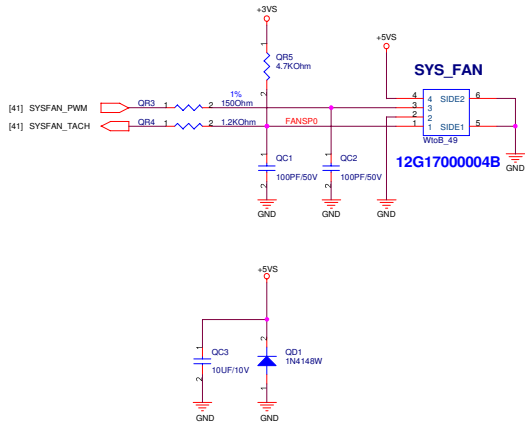


FA5/ SHBM

0: Disable Shared Memory with Host BIOS  
1: Enable Shared Memory with Host BIOS



System Fan Connector



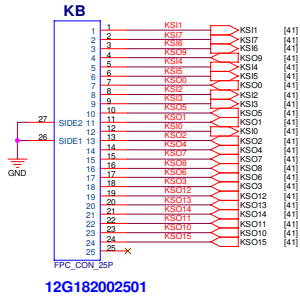
BIOS: 05G001204043

V1.1G

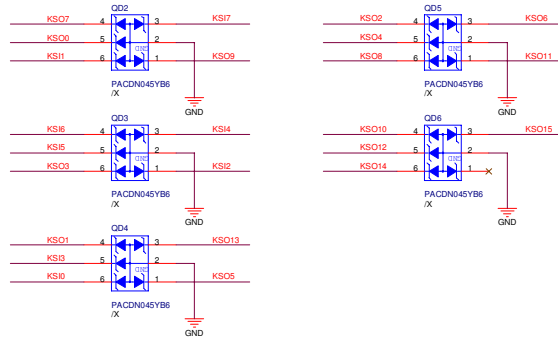
Z37S\_12



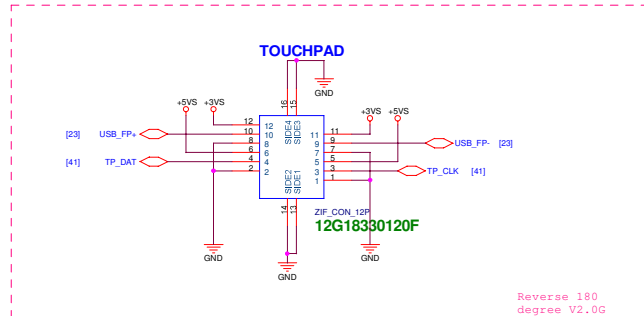
## Keyboard Connector



## FOR EMI/ESD



## Fingerprint & TouchPad Connector



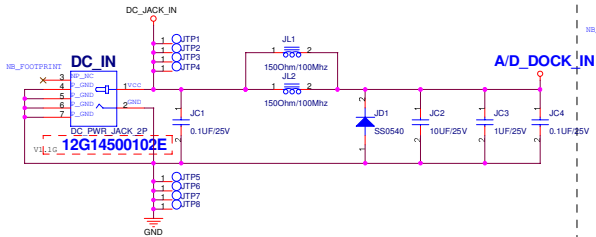
Z37S\_12



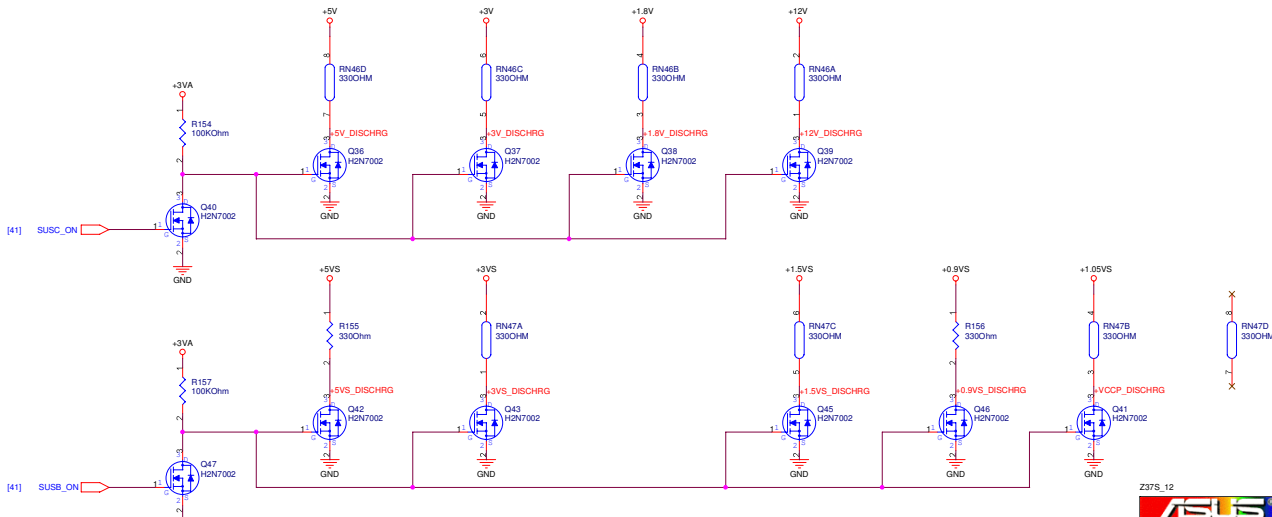
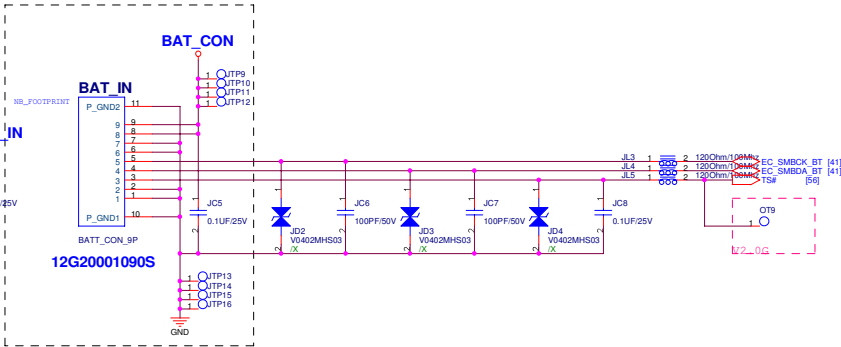




## DC-IN Connector



## BAT-IN Connector

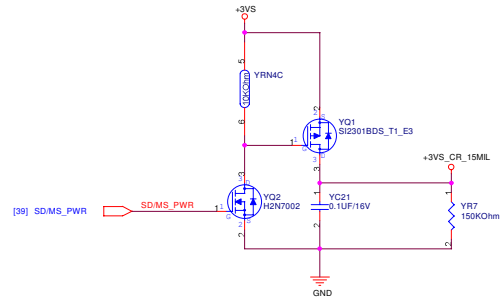


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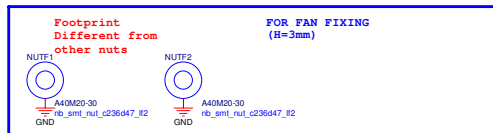
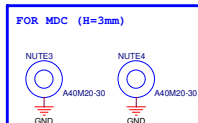
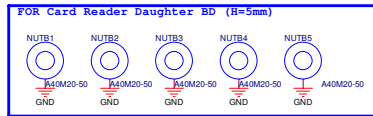
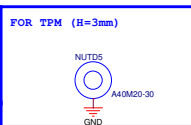
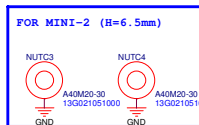
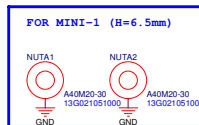


BTB08 CON 80P  
Blue CON 80P 0.8mm M.SMT  
12G160200804

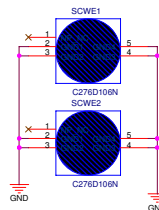
**BOM : 12G160200805 --8mmHigh**



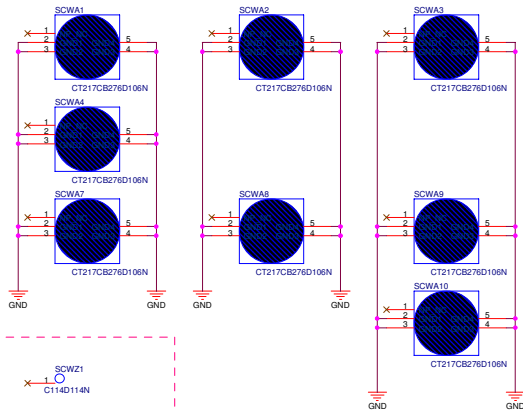




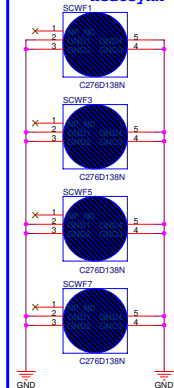
**Screw E**



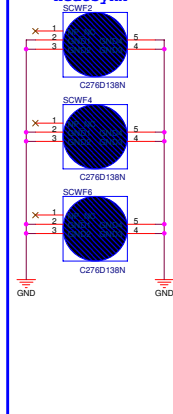
**Screw A**



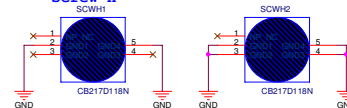
**Screw F CPU Heatsynk**



**NB GPU Heatsynk**



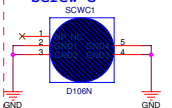
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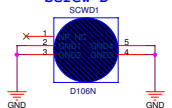
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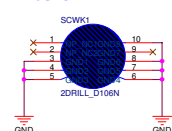
**Screw C**



**Screw D**



**Screw K**

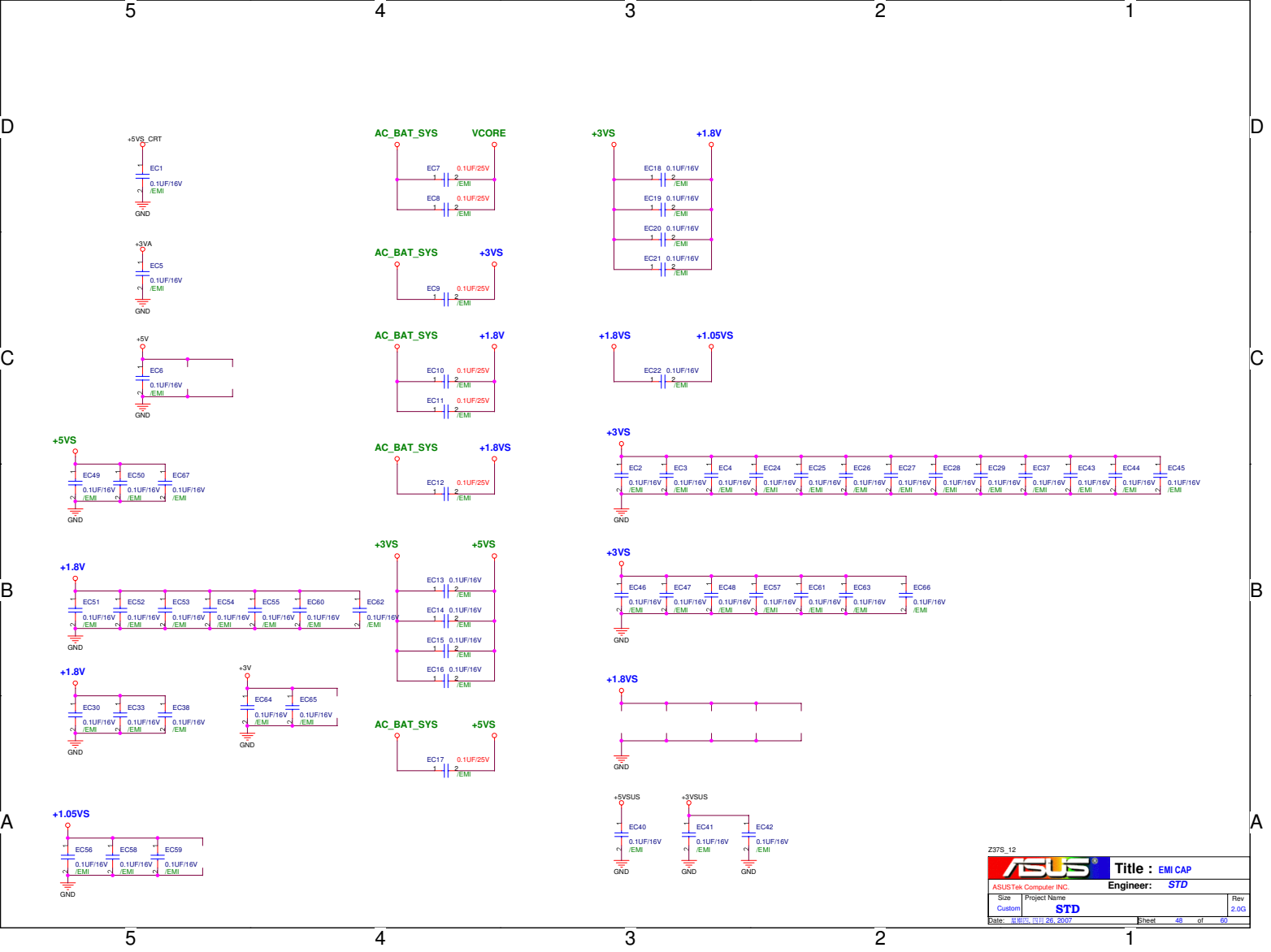


pin9 NC for 100mil space of RING

Z375\_12

<b>ASUS</b>		<b>Title : Screw Hole</b>	
ASUSTek Computer INC.		Engineer: STD	
Size	Project Name	Rev	2.03
Custom	STD		
Date: 2007.01.26	Sheet: 47	of 60	



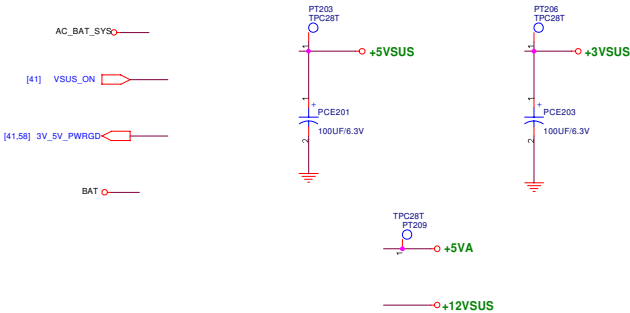






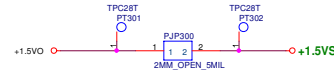
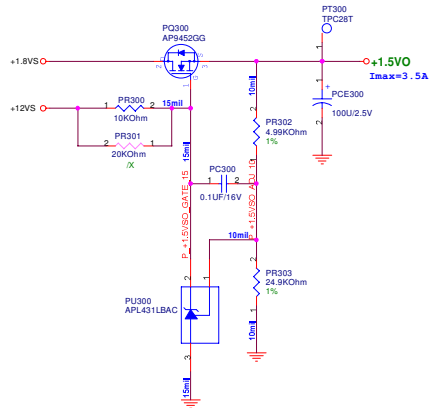


Put these elements close to daughter board !!





**+1.5VS / 3.5A**



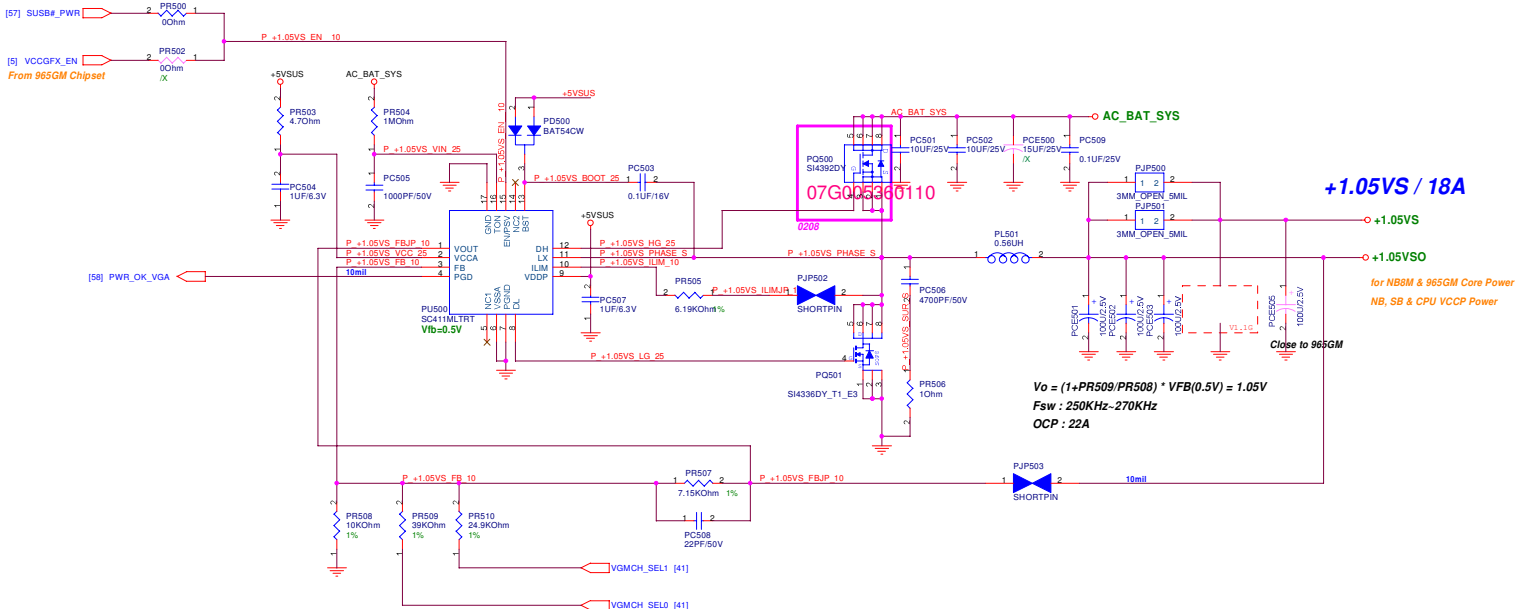
for CPU(VCCA), NB, SB, Other Devices Power







**Enable Signal :**  
 Implemet Intel 965GM --> PR502  
 Implemet NB8M Chipset --> PR500



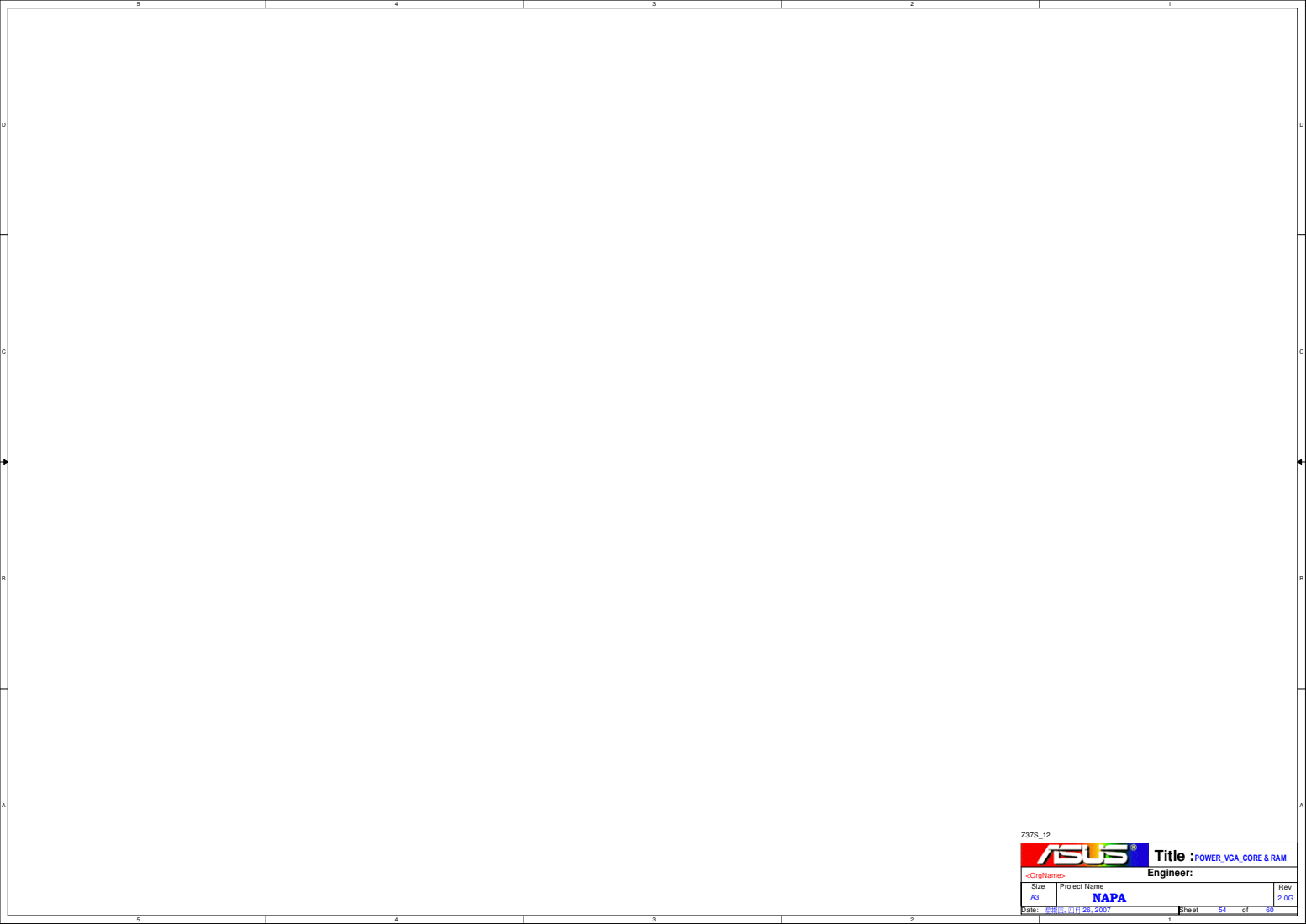
### +1.05VS

VGMCH_SELO	VGMCH_SEL1	Voltage
L	L	1.093V
X	L	1.001V
L	X	0.949V
X	X	0.857V

Z37S\_12

<b>ASUS</b>		<b>Title :</b> <Title>
ASUSTek COMPUTER Inc.		<b>Engineer:</b> Carl Chlou
Size	Project Name	Rev
A3	<Doc>	2.0G
Date: 2004.11.25.2007	Sheet	53 of 60





Z37S\_12



**Title :**POWER\_VGA\_CORE & RAM

<OrigName>

Size

Project Name

Rev

A3

**NAPA**

2.00

Date

Author

Checker

Drawn

of

Sheet

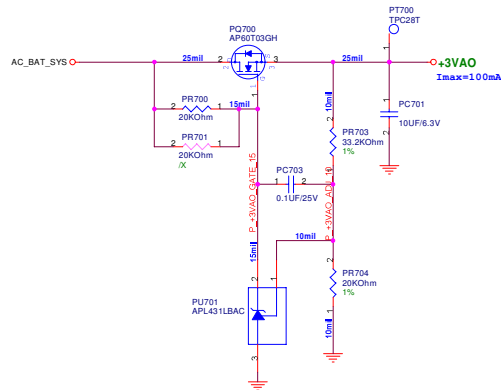
12/26/2007

54

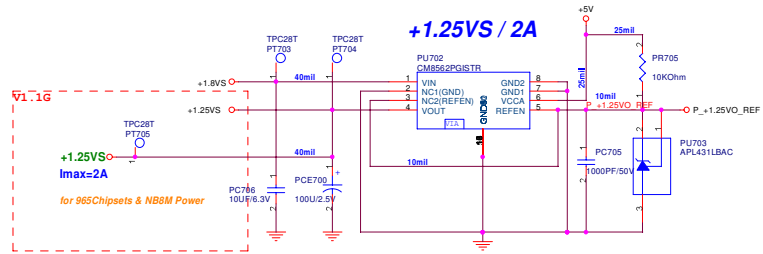
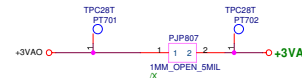
50

1





**+3VAO / 100mA**



**+1.25VS / 2A**

**+1.25VS**  
**I<sub>max</sub>=2A**  
for 965Chipsets & NB8M Power

Z378\_12

<b>ASUS</b>		<b>Title : POWER_I/O_+3VA &amp; +2.5V</b>	
-<OrgName>		<b>Engineer:</b>	
Size	Project Name	Rev	
A3	<b>NAPA</b>	2.0G	
Date: 2007.10.25	Sheet 55	of 60	

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[illegible]

VICTL < 0.8V or DCIN < 7V → Charger Disable

VICTL < 0.8V or DCIN < 7V → Charger Disable

<b>MODE ( Pin7 )</b>	<b>Battery</b>
High ( >2.6V )	4-Cell
Low ( <0.8V )	Battery Learn
High Impedance ( 1.6V < Vmode < 2V )	3-Cell

**Battery Charging Voltage :**  
 $+V_{BAT} = 3 \times [4.2235 + (V_{VCT} - 1.8) / 9.52]$

**Battery Charging Current :**  
 $I_{charge} = (0.075 / PR806) \times (V_{ictl} / 3.6)$

**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (0.075 / PR801) \times (V_{cls} / 4.2235)$

**Pre-Charging Mode :**

Precharging current = 127.1mA  
V<sub>ictl</sub> = 91.5mV

**Battery Cell Selection :**

BATSEL\_2P# = 1, 3 Cells; Vct1 = 1.074V  
=> Icharge = 1.491A  
BATSEL\_2P# = 0, 6 Cells; Vct1 = 1.81V  
=> Icharge = 2.514A

**Adaptor Max. Current :**

PR815 = 178K; I<sub>limit</sub> = 4.49A; 85.4W  
PR815 = 36K; I<sub>limit</sub> = 3.21A; 61.1W

[illegible]

AC\_APR\_UC = 1, Adaptor is present  
AC\_APR\_UC = 0, Adaptor is absent

### Battery Voltage



07G005450020

07G00535701

ECN EN-0034662  
STUFF

ECN EN-0034662  
STUFF

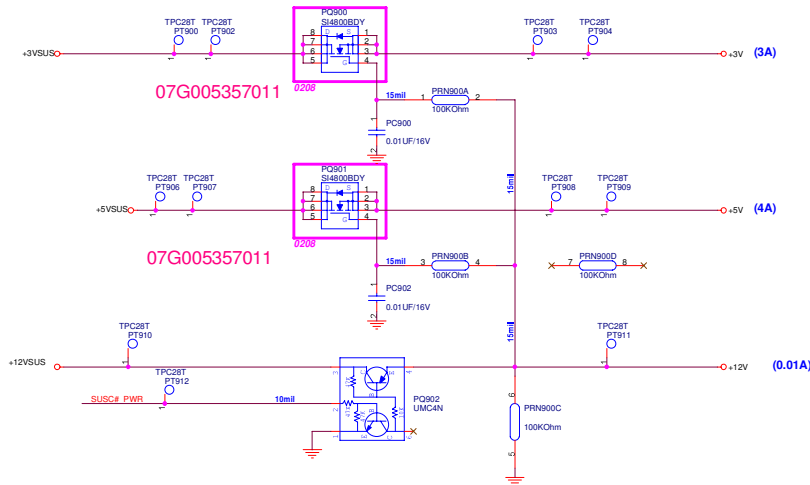
Z37S\_12



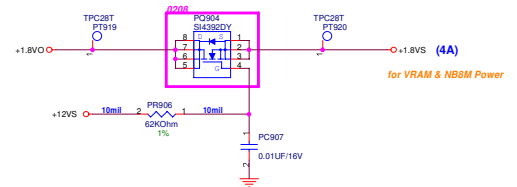
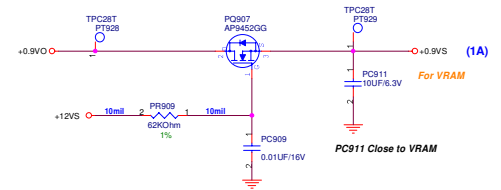
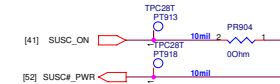
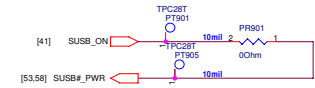
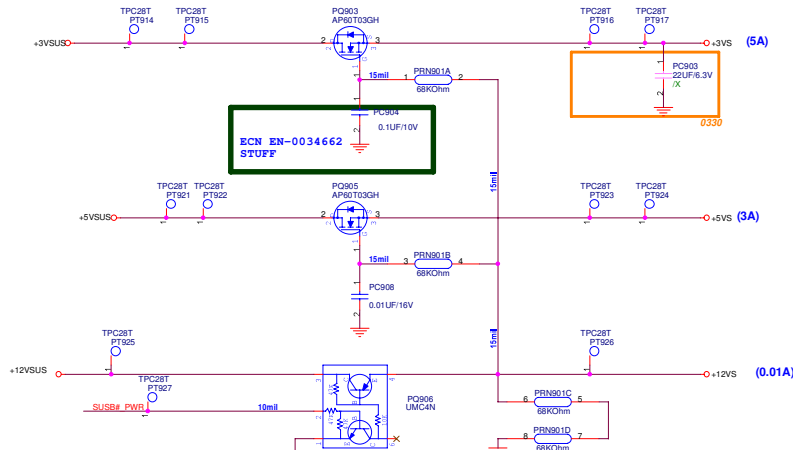
Size	Project Name
C	NAPA



## SUSC#\_PWR POWER



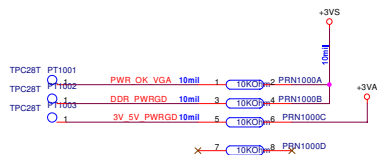
## SUSB#\_PWR POWER



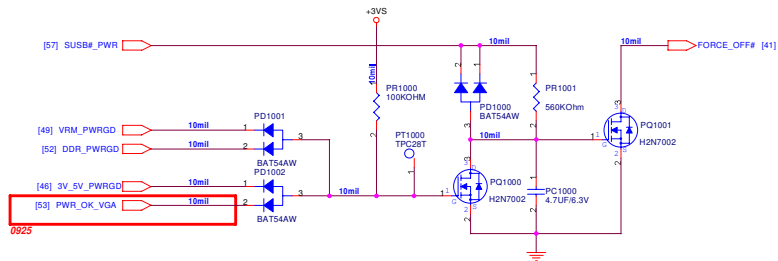
Z37S\_12

ASUS		Title : POWER_LOAD SWITCH	
Size		Engineer:	
Custom	Project Name	Rev	2.20
NAPA		Rev	
Date: 2007.11.26, 2007		Sheet 57 of 60	

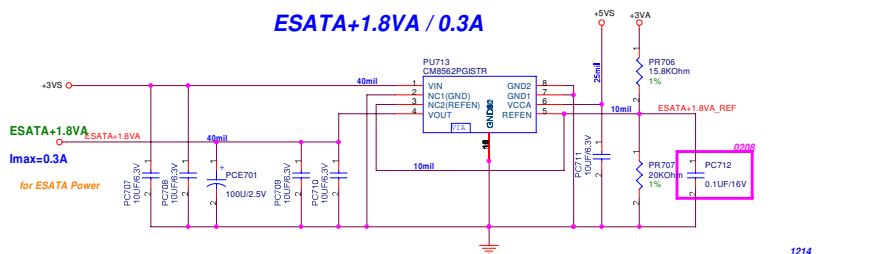




## Power Good Detector

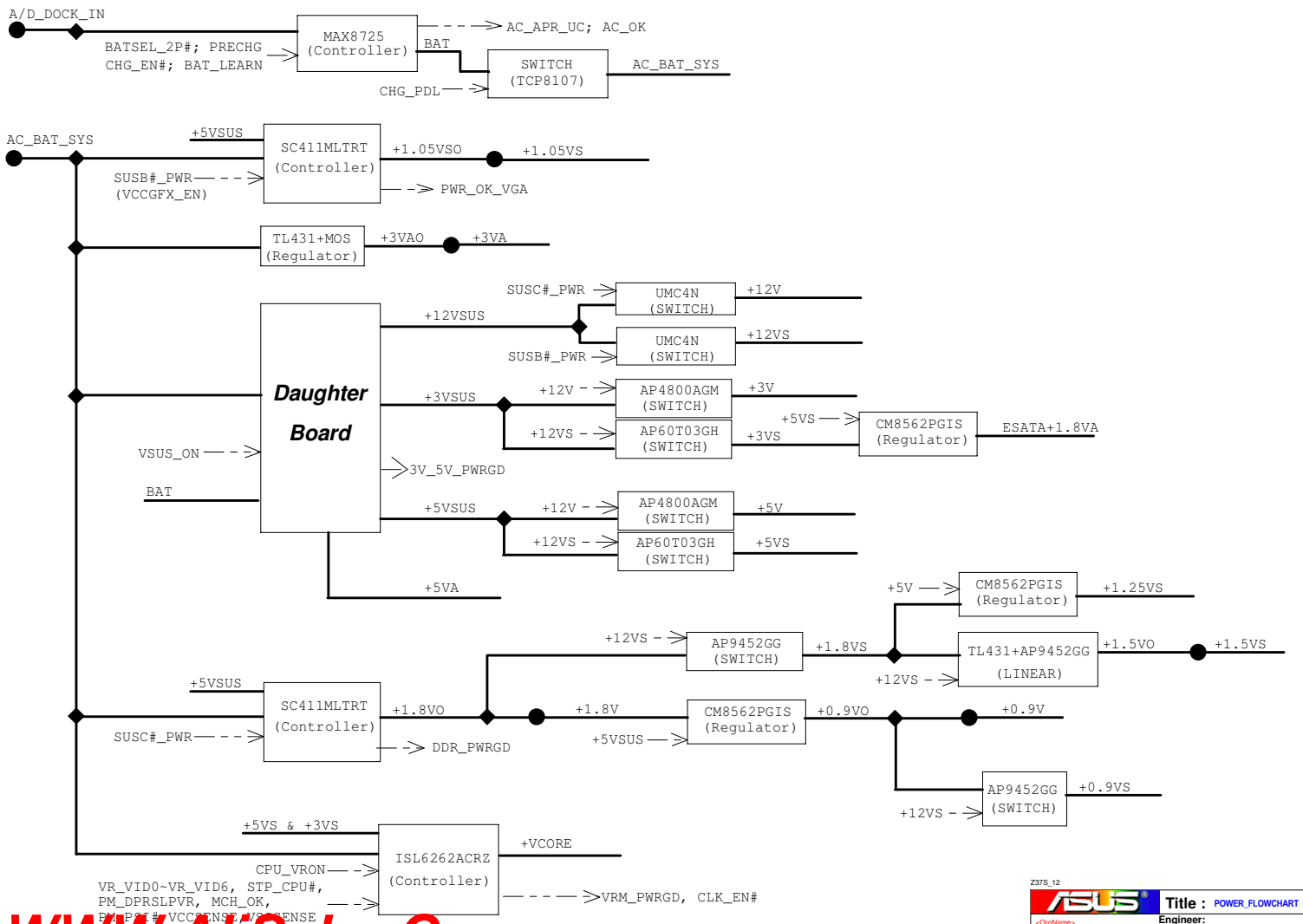


## ESATA+1.8VA / 0.3A



Z375\_12






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Z37S\_12

		<b>Title :</b> POWER_SIGNAL	
<OrigName>		<b>Engineer:</b> Carl_Chiou	
Size	Project Name	Rev	
Custom	NAPA	2.00	
Date	2007.12.26.2007	Sheet	60 of 60